OMRON USER'S MANUAL

Programmable Controller

Model SYSMAC-P0R

ONICS CO.

INTRODUCTION

"OMRON SYSMAC" is the trade name of OMRON's programmable controllers unparalleled in reliability and versatility.
Programmable controllers, which were initially developed to meet the demands by equipment manufacturing industries and large-scale plants for their production facilities, now answer the needs of industries from every field and have become original equipment for installation at factories.
The above trend has induced original equipment manufacturers to design the incorporation of programmable controllers in their machinery and equipment, and thus the demand for availability of the programmable controllers that can be handled as easily as components has been increasing. Accordingly, OMRON has sought to develop programmable controllers which are: a. small and economical, b. easy to handle by merely connecting a load and power and c. easy to operate by anyone at site, in addition to possessing flexibility that permits adapting to changes to the controlled systems or control parameters with simple keyboard operation and high reliability which can be materialized only by electronic control.
OMRON now offers with confidence the OMRON SYSMAC-P0R Package Type Programmable Controller, a first-class programmable controller with "CPU function" and "techniques responding adequately to the needs at every site." Programming with the SYSMAC-P0R can be performed easily and directly from ladder diagrams using the program console incorporated in the programmable controller.
The OMRON SYSMAC-P0 Step Advance Type Sequence Controller which employs the timing chart programming method is also recommended.

CONTENTS

1. Features

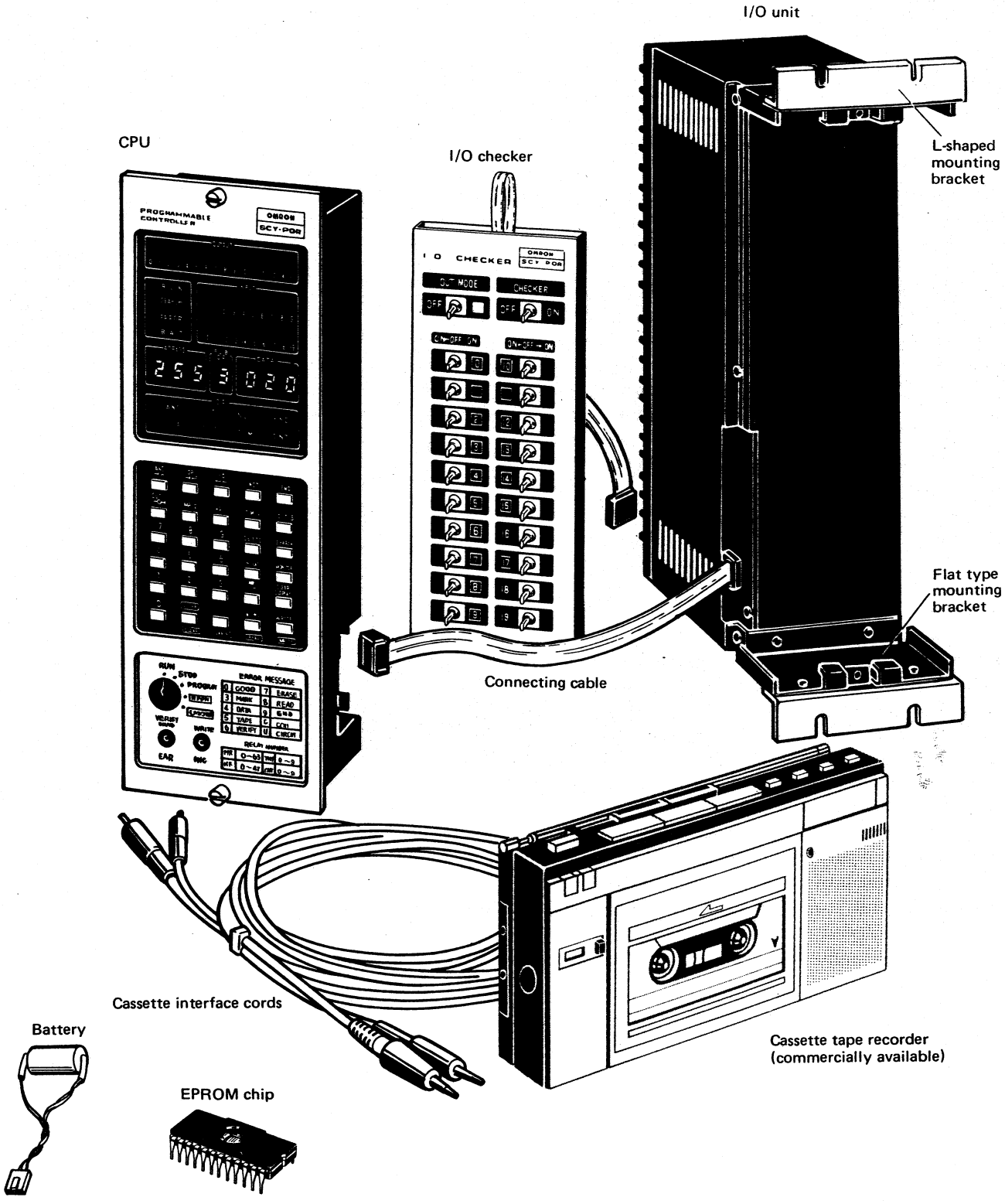
Compact, slim styled programmable controller with abundant checking functions and cassette tape adapter.

- **Integrated program console**
  The central processing unit (CPU) incorporates a program console which is provided with an abundance of operational check functions in addition to programming. From the keyboard of this program console, ladder diagrams can be programmed directly with ease and speed.
- **Continuity checking is possible according to the sequence of ladder diagram**
  The SYSMAC-P0R is capable of retrieving an instruction word (output instruction) during the program execution to check the circuit block concerned for electrical continuity according to the sequence of the ladder diagram. Furthermore, it monitors the present value of each timer or counter, thus facilitating the program simulation and maintenance operations of the controller.
- **RAM and RAM & ROM types for free selection**
  Normally, the RAM type programmable controller is supplied. However, the RAM & ROM type programmable controller is available for selection to meet the specifications of the equipment to be controlled. With the RAM & ROM type, a maximum of four program patterns can be written into the EPROM in units of 256 words per pattern. After the program writing, a user program can be selected for execution by operating the program console.
- **Flexible mounting style**
  Since the SYSMAC-P0R consists of a CPU and an I/O unit, the two units can be mounted either as an integrated unit or as separated units and wiring is also possible from either front or rear panel.
- **Built-in PROM writer function**
  The PROM writer function is incorporated only in the RAM & ROM type CPU to permit writing of a debugged program into the EPROM.
- **Programs can be recorded on cassette tape**
  By connection of the exclusive interface cords, programs in the CPU memory may be dumped onto a commercially available cassette tape.
- **Program address control is not required**
  Since direct programming from ladder diagrams is possible, the contents of the program memory are readily known through retrieval of instructions during program change, simulation, or maintenance. Therefore, it is not necessary to control the use of program addresses by coding sheets.

2. System Configuration and Specifications

2.1 Available Types

The SYSMAC-P0R consists of a central processing unit (CPU) and an I/O unit. As an optional accessory, an I/O checker for manual input is available for use in program debugging. A PROM writer and a cassette interface are contained in the CPU.



■ STANDARD TYPES

Classification	Components	Type
RAM type	RAM type CPU, I/O unit, Connecting cable (20cm), Battery, Mounting brackets (L-shaped/Flat type)	SCY-P0R10E
RAM & ROM type	RAM & ROM type CPU, I/O unit, Connecting cable (20cm), Battery, EPROM, Mounting brackets (L-shaped/Flat type)	SCY-P0R20E

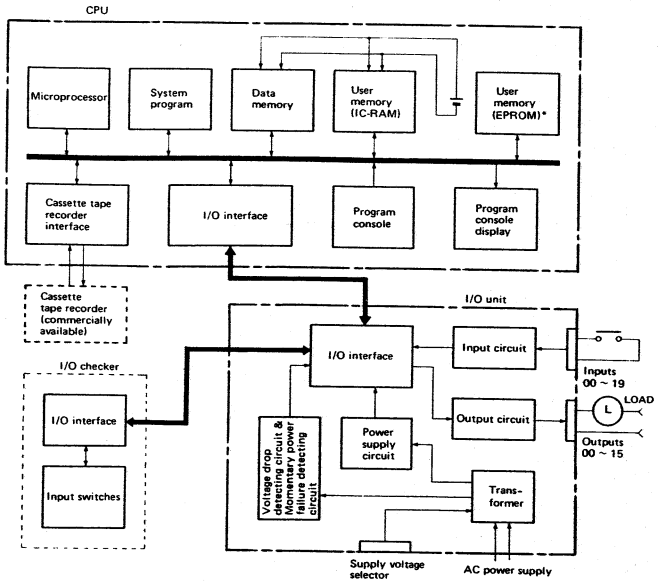
■ COMPONENTS AND OPTIONS (FOR SUPPLY INDIVIDUALLY)

Classification	Specification	Type
CPU	Program memory: IC-RAM with battery Weight: Approx. 1kg max.	SCYP0R-CPU10E
CPU	Program memory: IC-RAM with battery Weight: Approx. 1kg max. EPROM Weight: Approx. 1kg max.	SCYP0R-CPU20E
I/O unit	Weight: Approx. 4.6kg max.	SCYP0R-I/O01E
Connecting cable	For connection between CPU and I/O unit: 20cm Weight: Approx. 10g	SCYP0R-CN020
Connecting cable	For connection between CPU and I/O unit: 300cm Weight: Approx. 65g	SCYP0R-CN300
I/O checker	For program debugging Weight: Approx. 500g	SCYP0R-CHK01
Cassette interface cord	For connection between CPU and cassette tape recorder Weight: Approx. 50g	SCYP0R-PLG01
L-shaped mounting brackets	A pair of brackets supplied as a set Weight: Approx. 55g	SCYP0R-PAT01
Flat type mounting brackets	A pair of brackets supplied as a set Weight: Approx. 140g	SCYP0R-PAT02
EPROM chip*	Weight: Approx. 10g	ROM-F
Battery	3V lithium battery with connector Weight: Approx. 18g	SCY-BAT01

NOTE: * OMRON offers Type ROM-F (equivalent to 2716) developed under strict quality control as the EPROM (1K) chip for OMRON Programmable Controller series. Be sure to use this EPROM chip for the OMRON Programmable Controllers.

2.2 System Configuration

The system block diagram of the Type SCY-P0R20E (RAM & ROM type) is shown below.



NOTE: * Type SCY-P0R10E (RAM type) is not provided with a user memory (EPROM).

2.3 Specifications

■ RATINGS

Supply voltage	AC 110, 120, 220, or 240V, 50/60Hz*
Operating voltage range	85 to 110% of rated voltage**
Power consumption	55VA max.
Insulation resistance	20MΩ min. at DC 500V (between external terminal and outer casing)
Dielectric strength	AC 1,500V, 50/60Hz for 1 minute (between external terminal and outer casing)
Noise immunity	1,000Vp-p Rise time: 1nsec; Pulse width: 2μsec
Vibration resistance	16.7Hz, 3-mm double amplitude for 2 hrs.
Shock resistance	10G's (in X, Y, Z directions, respectively 3 times)
Ambient temperature	Operating: 0 to +50°C Storage: −10 to +70°C
Humidity	30 to 90% RH (without condensation)
Ambient atmosphere	Must be free from corrosive gases
Grounding	Package type (CPU and I/O unit are separable)
Enclosure	CPU sides: Dark gray CPU front: Aluminum hairline process I/O unit: Dark gray
Weight	CPU: 1.1kg max. I/O unit: 4.6kg max.

NOTE: * Set the voltage selector socket to the required voltage.
** A momentary power failure of less than ½ cycle is ignored by the programmable controller. If a momentary power failure of ½ to 1 cycles occurs, the power failure condition may or may not be detected by the programmable controller since it is in an unstable area. If a power failure of more than 1 cycle occurs, the programmable controller detects the power failure.

■ CHARACTERISTICS

Control system	Stored program system
Main control element	LSI, TTL, C-MOS
Programming system	Ladder diagram
Instruction word length	16 bits/word
Number of instructions	13 kinds
Scan time	21msec max./256 words
Programming capacity	RAM: 256 words EPROM: 256 words x 4
Number of input points	20 points (Relay Nos. 00 ~ 19)
Number of output points	16 points (Relay Nos. 00 ~ 15)
Number of internal auxiliary relays	59 points (Relay Nos. 00 ~ 58)
Number of special auxiliary relays	5 points (Relay Nos. 59 ~ 63) • 59: Turns ON for 1 scan time when power is applied • 60: 0.1sec clock • 61: 1sec clock • 62: Turns ON when the battery is abnormal • 63: Turns ON when the memory is abnormal
Number of latching relays	47 points (Relay Nos. 00 ~ 46)
Number of latching auxiliary relays	1 point (Relay No. 47) When relay No. 47 is set, all outputs are inhibited and the output display goes out.
Number of timers and counters	10 points (Relay Nos. 0 ~ 9) respectively Timer: 0.1 ~ 25.5sec Counter: 1 ~ 255 counts
Timer accuracy	(Set value x ±1%) + (±50msec)
Counter response speed	10Hz max.
Memory protection function during power failure	Status data of respective latching relays and counters before the power failure are retained in the memory.
Diagnostic function	Memory failure (Sum check) CPU failure (Watchdog timer) Battery failure (Battery not loaded, battery voltage drop) Program check • Coil duplication check • END instruction check • Circuit error check (syntax check)

■ INPUT

Input form	No-voltage contact input (photocoupler isolation)
Input voltage	DC 20V (built-in power supply)
Input current	10mA
Input operating level	ON: 5mA min. OFF: 2mA max.
Input response speed	7 to 14msec
Input impedance	1.8kΩ
Input points/common (terminal block connection)	10 points/common (terminal block connector)
Operation indication	LED's on the front panel of the CPU (The corresponding LED illuminates when the input is ON.)

■ OUTPUT

Output form	Relay (SPST-NO) contact output (no-voltage)
Relay	OMRON Type MY2*
Contact rating	DC 30V/AC 250V 2A, resistive load DC 30V/AC 250V 0.8A, inductive load
Output points/common (terminal block connection)	4 points/common (terminal block connector)**
Operation indication	LED's on the front panel of the CPU (The corresponding LED illuminates when the output is ON.)

NOTES: * Interchangeable with OMRON Model G3F solid-state relay.
** 7A max. per common terminal.

■ DIAGNOSTIC FUNCTIONS

As the diagnostic functions of the SYSMAC-P0R, checks on the items listed in the following tables are performed in the PROGRAM and RUN modes, respectively.

• PROGRAM mode

Diagnostic function / Item	Function	Error indication	Error code indication
Program check: Coil duplication check	Checks coil numbers for duplication.	ON	C
Program check: END instruction check	Checks the presence of END instruction at the end of the program.	ON	9
Program check: Circuit error check	Checks the ladder diagram for proper configuration.	ON	U
Program check: Program over check	Checks if the number of program instructions exceeds the memory capacity (i.e., 256 words) in Insert operation.	–	–

NOTE: In the "Program Over" condition, entries by the Insert key will be ignored.

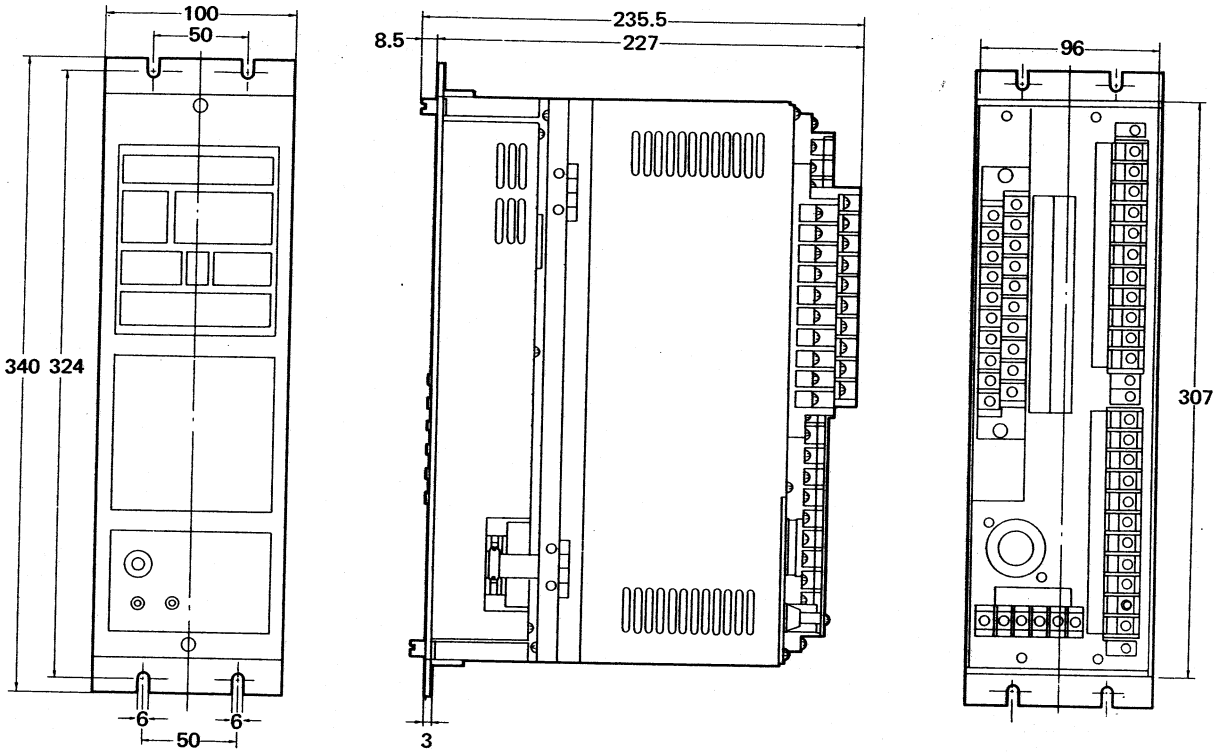
- **RUN mode**

Item	Diagnostic function		Indication		State of program execution	Special internal auxiliary relay
		CPU failure indicator	RUN indicator	BAT indicator		
Program memory	Sum check	ON	Flashes ON/OFF	–	Continue	MR63: ON
Lithium battery*	Rated voltage check Battery loading check	–	ON	ON	Continue	MR62: ON
CPU failure	Watchdog timer	ON	OFF	–	Stop (all outputs will be turned OFF)	–

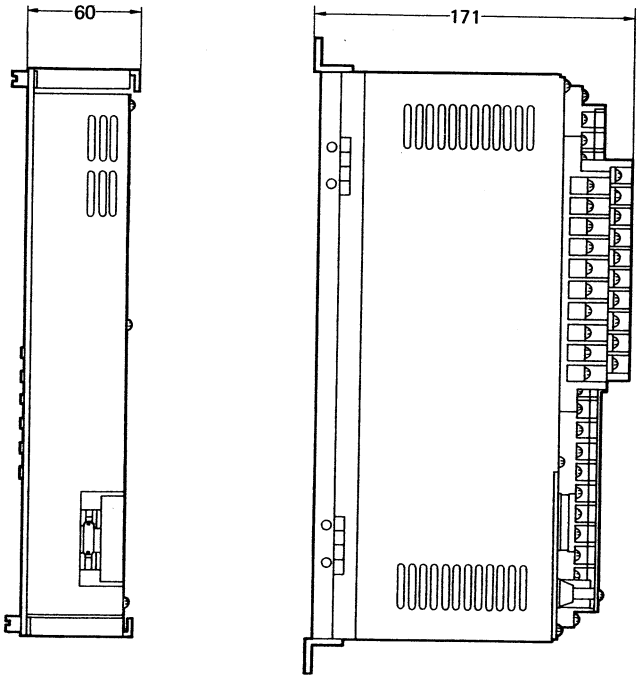
NOTE: * The lithium battery checks are performed in all the modes. After the BAT indicator illuminates, be sure to replace the battery within a week, or the contents of the program memory will be destroyed.

2.4 Dimensions

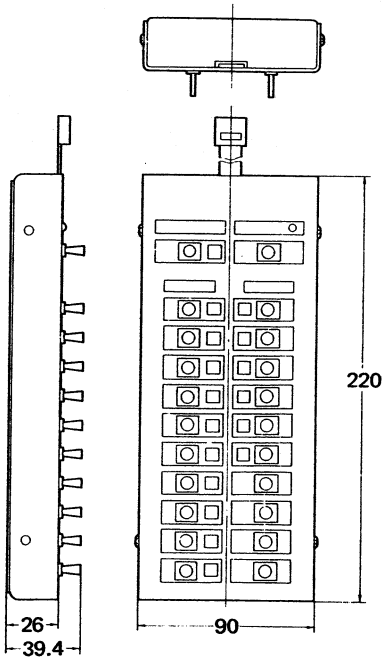
- **Programmable controller (with CPU and I/O unit integrated)**



- **Programmable controller (with CPU and I/O separated)**

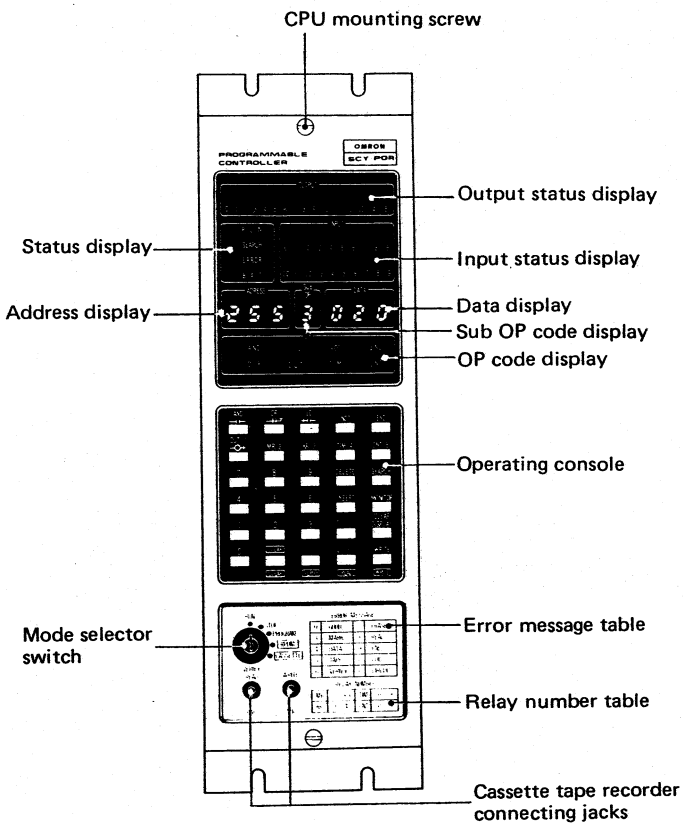


- **I/O checker**

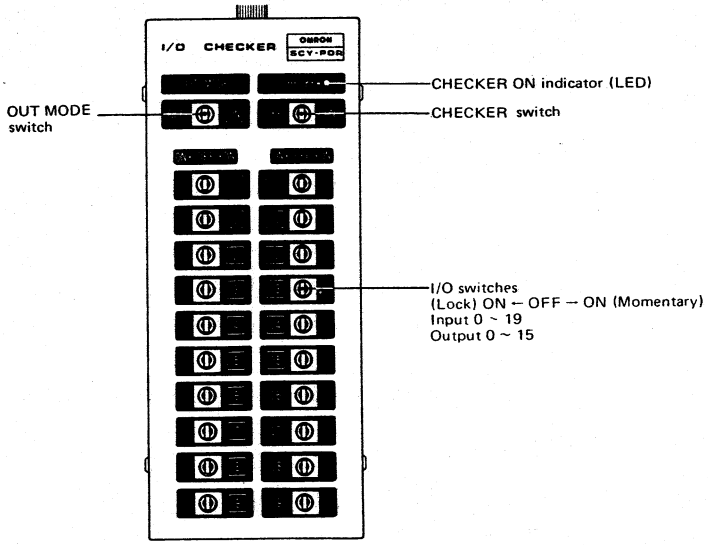


2.5 Names of Respective Parts

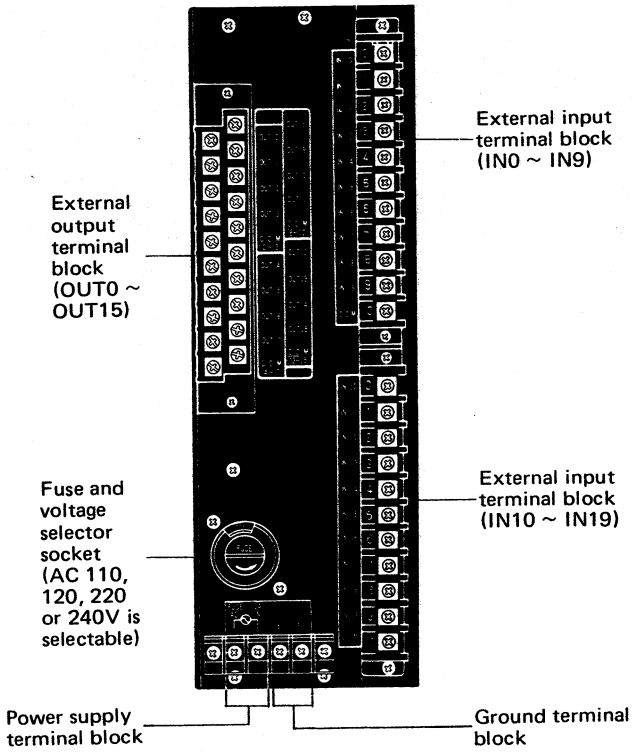
- **Front panel of CPU**



- **I/O checker**



- **Rear panel of I/O unit**



3. Assignment of Relay Numbers

Relay numbers correspond to the data memory areas and the operation (ON/OFF state) of each relay is stored in the corresponding memory area.
The method of assigning relay numbers used for the SYSMAC-P0R is as follows.

3.1 List of Relay Numbers

Name	No. of points	Relay number
Input relay	20	00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 16 17 18 19
Output relay	16	00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15
Internal auxiliary relay	59	00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58
Latching relay	40	00 01 02 03 04 05 06 07 08 09 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46
Timer	10	0 1 2 3 4 5 6 7 8 9
Counter	10	0 1 2 3 4 5 6 7 8 9

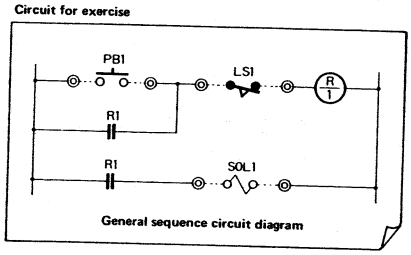
Name	No. of points	Relay number	Description
Special auxiliary relay	5	59	This relay operates for 1 scan time when power is applied.
		60	This relay is used for 0.1sec clock.
		61	This relay is used for 1sec clock.
		62	This relay operates when a battery failure occurs.
		63	This relay operates when a memory failure occurs.
Special latching relay	1	47	When this relay operates, all output are inhibited and all output indicators go out.

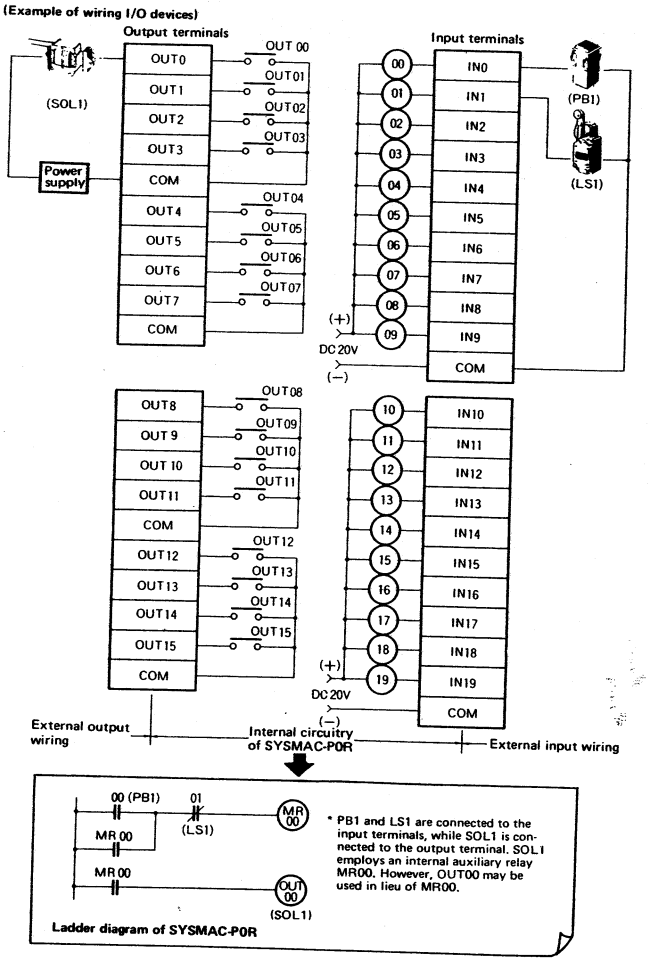
- With the SYSMAC-P0R, relay numbers other than above cannot be used. For setting the timer and counter values, values higher than 255 cannot be used.

3.2 Determination of I/O Relay Numbers

1. In a sequence circuit diagram which is generally known, a sequence circuit is drawn with input/output devices included and I/O device symbols and relay numbers are arbitrarily determined. However, since the SYSMAC-P0R cannot recognize such arbitrary I/O device symbols and relay numbers, it is necessary to determine the I/O terminals to which I/O devices are to be connected.

2. The ladder diagrams of the SYSMAC-P0R require the relay numbers corresponding to the I/O devices. The relay numbers are determined by the locations (I/O terminals) of I/O terminal blocks to which the I/O devices are connected. Each of these relay numbers must be used for ladder diagrams and programming.





3.3 Determination of Internal Auxiliary Relay Numbers

The SYSMAC-P0R has 59 internal auxiliary relays which are used for internal data transfer. They are independent of I/O devices in sequence. Since the internal auxiliary relays are the data memories incorporated in the CPU, no wiring to the I/O terminals is required. (In other words, they cannot be used as contact outputs.)

- **Internal auxiliary relay numbers**

00	01	02	03	04	05	06	07	08	09
10	11	12	13	14	15	16	17	18	19
20	21	22	23	24	25	26	27	28	29
30	31	32	33	34	35	36	37	38	39
40	41	42	43	44	45	46	47	48	49
50	51	52	53	54	55	56	57	58	

NOTES: 1. Relay numbers 00 ~ 58 may not necessarily be assigned consecutively.
2. When using an internal auxiliary relay, the letters "MR" must be prefixed to the relay number (e.g. MR00).
3. Relay coil number cannot be used in duplication. However, the number of relay contacts is not limited for use.
4. If more than 59 internal auxiliary relays are required, output relay numbers of the output terminals to which output devices are not connected may be used as internal auxiliary relay numbers.

3.4 Determination of Special Auxiliary Relay Numbers

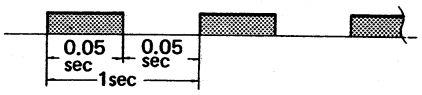
5 special auxiliary relays are provided. These relays are sort of internal auxiliary relays which operate and release according to the internal conditions controlled by hardware and are independent of the I/O devices in sequence.

- **Special auxiliary relay numbers**

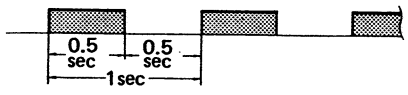
59	60	61	62	63

59: This relay operates for 1 scan time when the mode selector switch is changed from STOP to RUN after power application in the RUN mode. Use of this relay is recommended to generate a signal to reset latching relays, counters, etc. upon power application.

60: This relay is used to generate 0.1sec clock. When used in conjunction with a counter, it functions as a timer for memory retention during a power failure. The relay output can also be used as a flicker signal.



61: This relay is used to generate 1sec clock. When used in conjunction with a counter, it functions as a timer for memory retention during a power failure. The relay output can also be used as a flicker signal.



62: This relay operates when a battery failure occurs and releases when the battery is returned to normal. When this relay operates, the BAT indicator on the front panel of the CPU illuminates. These relay outputs cannot be transmitted directly to an output terminal. If any of the relay outputs is desired to be transmitted externally, prepare and program a circuit so that the relay output is transmitted externally through an output relay. (Refer to paragraph 5.2.5, Applied Programs.)

63: This relay operates when a memory failure occurs. To release this relay, change the mode selector switch position or turn off the power. These relay outputs cannot be transmitted directly to an output terminal. If any of the relay outputs is desired to be transmitted externally, prepare and program a circuit so that the relay output is transmitted externally through an output relay. (Refer to paragraph 5.2.6, Applied Programs.)

NOTES: 1. When using any special auxiliary relay, the letters "MR" must be prefixed to the relay number (e.g., MR59).
2. Special auxiliary relays cannot be used as output relays. However, the number of these relay contacts is not limited for use.

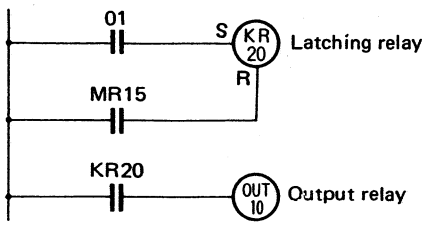
3.5 Determination of Latching Relay Numbers

The SYSMAC-P0R has 47 latching relays whose operating states before a power failure can be retained in the memory. Since the operating states of these relays are stored in the memory, all their outputs at the time of the power failure are turned off, but the relays will return to the state before the power failure when power is applied again. Memory retention time after a power failure is about 2 years just the same as that of the program memory.

- **Latching relay numbers**

00	01	02	03	04	05	06	07	08	09
10	11	12	13	14	15	16	17	18	19
20	21	22	23	24	25	26	27	28	29
30	31	32	33	34	35	36	37	38	39
40	41	42	43	44	45	46			

NOTES: 1. Relay numbers 00 ~ 46 may not necessarily be assigned consecutively.
2. When using a latching relay, the letters "KR" must be prefixed to the relay number.
3. Relay coil numbers cannot be used in duplication. However, the number of relay contacts is not limited for use.
4. When set and reset input signals are applied simultaneously, the reset input signal takes precedence over the set input signal.
5. These relay outputs cannot be transmitted directly to an output terminal. If any of the relay outputs is desired to be transmitted externally, prepare and program a circuit so that the relay output is transmitted externally through an output relay.



3.6 Determination of Special Latching Relay Number

The SYSMAC-P0R has only one special latching relay whose relay number is KR47. When the KR47 operates, all output relays are disabled, causing their outputs to turn off and all the operation indicators of the output relays to be extinguished. At this time, the RUN indicator flashes. When the KR47 releases, the output relays are put in the ON or OFF state depending on the program conditions at that time, causing the operation indicators of the output relays to be illuminated or extinguished accordingly. At this time, the RUN indicator changes from the flashing state to the illuminated state.

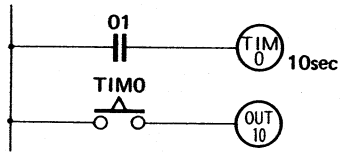
3.7 Determination of Timer Numbers

The SYSMAC-P0R has 10 timers which are used for timer numbers in programming.

- **Timer numbers**

0	1	2	3	4	5	6	7	8	9

NOTES: 1. Timer numbers 0 ~ 9 may not necessarily be assigned consecutively.
2. When using a timer, the letters "TIM" must be prefixed to the timer number (e.g., TIM0).
3. Timer coil numbers cannot be used in duplication. However, the number of timer contacts is not limited for use.



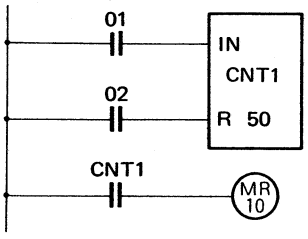
3.8 Determination of Counter Numbers

The SYSMAC-P0R has 10 counters which are used as counter numbers in programming.

- **Counter numbers**

0	1	2	3	4	5	6	7	8	9

NOTES: 1. Counter numbers 0 ~ 9 may not necessarily be assigned consecutively.
2. When using a counter, the letters "CNT" must be prefixed to the counter number (e.g., CNT1).
3. Counter coil numbers cannot be used in duplication. However, the number of counter contacts is not limited for use..

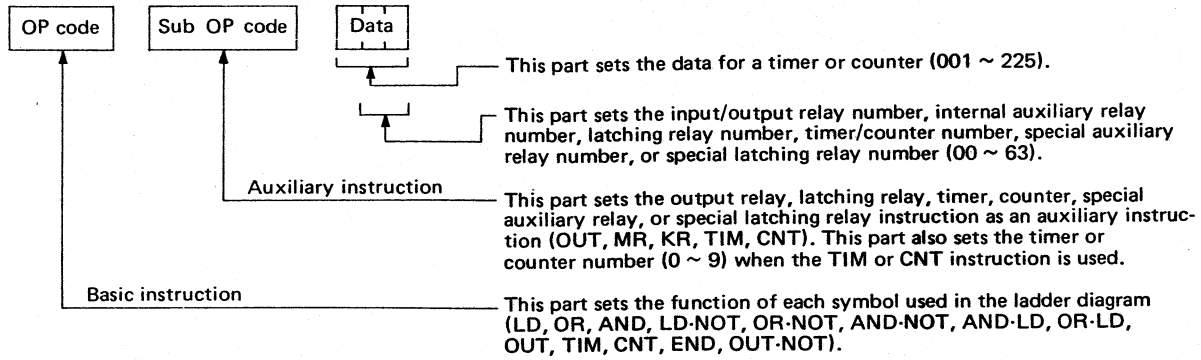


4. Instruction Words

A sequence circuit is programmed according to the ladder diagram instruction words provided for the SYSMAC-P0R. In this chapter, usages of ladder diagrams and ladder diagram instruction words are described.

4.1 Configuration of Instruction Words

Each instruction word used in the SYSMAC-P0R consists of the following 3 blocks.



4.2 List of Instructions

- **Basic instructions (OP codes)**

No.	Instruction	Symbol	Function	Data
1	LOAD	LD	Logical start operation.	Input relays 00 ~ 19 Output relays 00 ~ 15 Internal auxiliary relays 00 ~ 58 Latching relays 00 ~ 46 Timers 0 ~ 9 Counters 0 ~ 9 Special auxiliary relays 59 ~ 63 Special latching relay 47
2	LOAD NOT	LD NOT	Logical NOT start operation.	
3	AND	AND	Logical AND operation.	
4	AND NOT	AND NOT	Logical AND NOT operation.	
5	OR	OR	Logical OR operation.	
6	OR NOT	OR NOT	Logical OR NOT operation.	
7	AND LOAD	AND LD	Logical AND operation with the condition of the preceding block.	——
8	OR LOAD	OR LD	Logical OR operation with the condition of the preceding block.	
9	OUT	OUT/1	Outputs the result of a logical operation to the specified output relay, internal auxiliary relay, or latching relay.	Output relays 00 ~ 15 Internal auxiliary relays 00 ~ 58 Latching relays 00 ~ 46
10	OUT NOT	OUT/1 NOT	Inverts the results of a logical operation and then outputs them to the specified output relay, internal auxiliary relay or latching relay.	
11	TIMER	TIM/4	On-delay timer operation.	Timer Nos. 0 ~ 9 Counter Nos. 0 ~ 9 Setting value 001 ~ 255
12	COUNTER	CNT/5	Down counter operation.	
13	END	END	The end of a program.	——

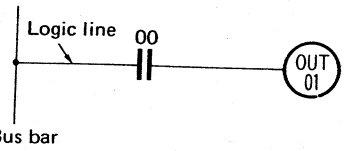
- **Auxiliary instructions (Sub OP codes)**

No.	Instructions	Symbol	Function	Data
1	Internal auxiliary relay	MR/2	Indicates an internal auxiliary relay.	Internal auxiliary relays 00 ~ 58
2	Latching relay	KR/3	Indicates a latching relay	Latching relays 00 ~ 46

4.3 Explanation of Instruction Words

■ LOAD (LD) & OUTPUT (OUT) INSTRUCTIONS

If each logic line starts with an NO contact, use the LD instruction. Use the OUT instruction for a relay coil.



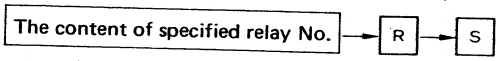
Coding

Address	OP	Sub OP	Data
000	LD		00
001	OUT		01

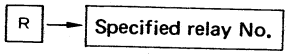
Contents of Registers

R	S
00	—
00	—

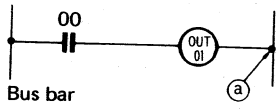
- **Operation of each register**
  The LD instruction causes the content (ON or OFF state) of the specified relay number to be stored into the RESULT REGISTER (hereafter referred to as "R register"). It also causes the previous result in the R register to be transferred to the STACK REGISTER (hereafter referred to as "S register").



The OUT instruction causes the content of the R register to be output to the specified relay number. In this case, the content of the R register will remain unchanged.

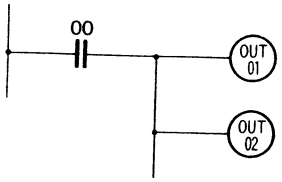


- Bus bar of a different phase is not required to be programmed.



Connection to the bus bar of a different phase (part ⓐ) is accomplished automatically by programming an OUT instruction.

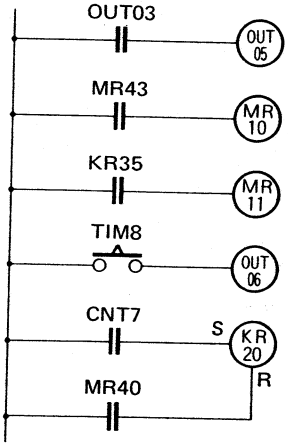
- **Consecutive OUT instructions**
  If the OUT instruction is followed by another OUT instruction, this condition is regarded as a circuit error during the program check. However, each output relay operates normally.



Coding

OP	Sub OP	Data
LD		00
OUT		01
OUT		02
⋮	⋮	⋮

- The LD instruction is used for any NO contact at the start of each logic line.



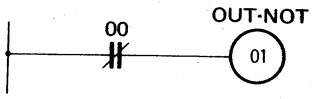
Coding

OP	Sub OP	Data
LD	OUT/1	03
OUT		05
LD	MR/2	43
OUT	MR/2	10
LD	KR/3	35
OUT	MR/2	11
LD	TIM/4	8
OUT		06
LD	CNT/5	7
LD	MR/2	40
OUT	KR/3	20
⋮	⋮	⋮

- The OUT instruction is used when an output relay, internal auxiliary relay, or latching relay is employed.

■ LOAD NOT (LD·NOT) & OUTPUT NOT (OUT·NOT) INSTRUCTIONS

If each logic line starts with an NC contact, use the LD·NOT instruction in lieu of the LD instruction. Use the OUT·NOT instruction to invert the output condition.



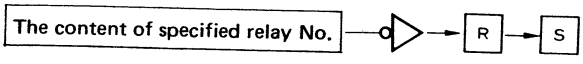
Coding

Address	OP	Sub OP	Data
000	LD·NOT		00
001	OUT·NOT		01

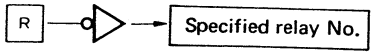
Contents of Registers

R	S
00	—
00	—

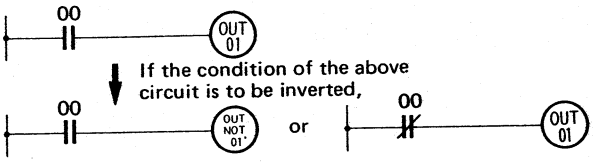
- **Operation of each register**
  The LD·NOT instruction causes the content of the specified relay number to be inverted and then stored into the R register.



The OUT·NOT instruction causes the content of the R register to be inverted and then output to the specified relay number. In this case, the content of the R register will remain unchanged.

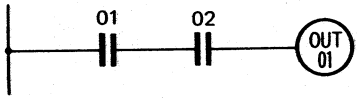


- The LD·NOT instruction is used for any NC contact at the start of each logic line.
- The OUT·NOT instruction may be used when an output relay, internal auxiliary relay, or latching relay is employed.
- Normally, the OUT·NOT instruction is not used. However, the instruction may be applied in the following case.



■ AND INSTRUCTION

NO contacts in series are processed by the AND instruction.



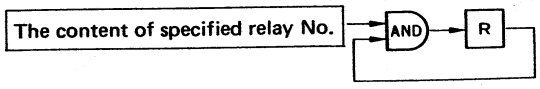
Coding

Address	OP	Sub OP	Data
000	LD		01
001	AND		02
002	OUT		01

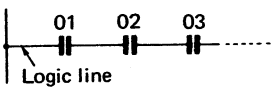
Contents of Registers

01	—
01 02	—
01 02	—

- **Operation of each register**
  The AND instruction causes the logical AND operation to be performed between the content of the specified relay number and the content of the R register. The result of the logical AND operation will be newly stored in the R register.



- **Number of contacts**
  The number of contacts is not limited for use on a logic line. As many NO contacts as required can be connected by means of the [AND] key.

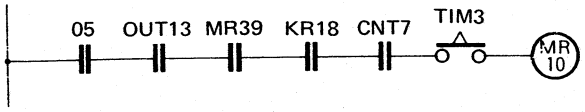


Coding

Address	OP	Sub OP	Data
	LD		01
	AND		02
	AND		03
	⋮		⋮

In this case, the contact of the first relay number 01 is at the start of each logic line. Therefore, the relay contact must be programmed as "LD01."

- The AND instruction is a series connection instruction and is used when all the contacts to be connected in series are NO contacts.

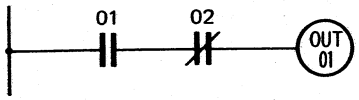


Coding

OP	Sub OP	Data
LD		05
AND	OUT/1	13
AND	MR/2	39
AND	KR/3	18
AND	CNT/5	7
AND	TIM/4	3
OUT	MR/2	10

■ AND NOT INSTRUCTION

If an NC contact is connected in series, use the AND·NOT instruction in lieu of the AND instruction.



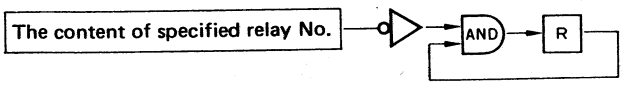
Coding

Address	OP	Sub OP	Data
000	LD		01
001	AND·NOT		02
002	OUT		01

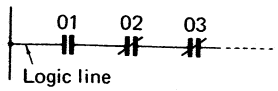
Contents of Registers

01	—
01 02	—
01 02	—

- **Operation of each register**
  The AND·NOT instruction causes the content of the specified relay number to be inverted and then ANDed with the content of the R register. The result of the logical AND operation will be newly stored in the R register.



- **Number of contacts**
  The number of contacts is not limited for use on a logic line. As many NC contacts as required can be connected in series by means of [AND] [NOT] keys.



Coding

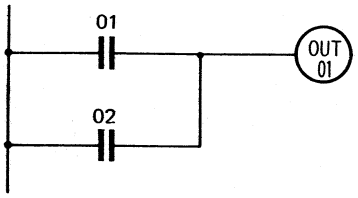
LD		01
AND-NOT		02
AND-NOT		03
⋮		⋮

In this case, the contact of the first relay number 01 is at the start of each logic line. Therefore, the relay contact must be programmed as "LD01."

- The AND-NOT instruction is a series connection instruction and is used when all the contacts to be connected in series are NC contacts.

■ OR INSTRUCTION

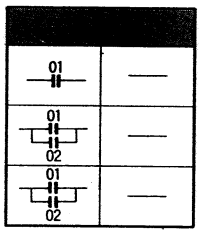
NO contacts in parallel are processed by the OR instruction.



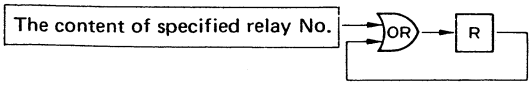
Coding

000	LD		01
001	OR		02
002	OUT		01

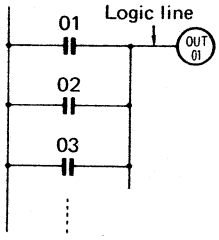
Contents of Registers



- **Operation of each register**
  The OR instruction causes the logical OR operation to be performed between the content of the specified relay number and the content of the R register. The result of the logical OR operation will be newly stored in the R register.



- **Number of contacts**
  The number of contacts is not limited for use on a logic line. As many NO contacts as required can be connected by means of [OR] key.



Coding

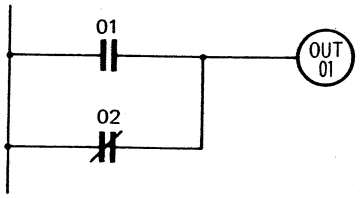
LD		01
OR		02
OR		03
⋮		⋮
OUT		01

In this case, the contact of the first relay number 01 is at the start of each logic line. Therefore, the relay contact must be programmed as "LD01."

- The OR instruction is a parallel connection instruction and is used when all the contacts to be connected in parallel are NO contacts.

■ OR-NOT INSTRUCTION

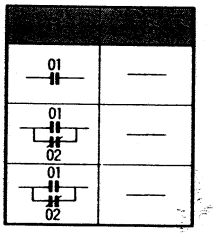
If an NC contact is to be connected in parallel, use the OR-NOT instruction in lieu of the OR instruction.



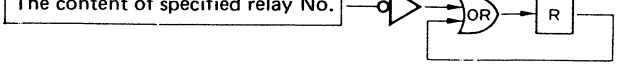
Coding

000	LD		01
001	OR-NOT		02
002	OUT		01

Contents of Registers

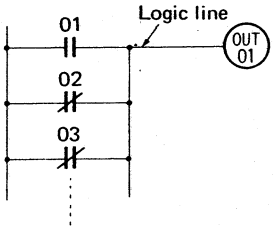


- **Operation of each register**
  The OR-NOT instruction causes the content of the specified relay number to be inverted and then ORed with the content of the R register. The result of the logical OR operation will be newly stored in the R register.



- **Number of contacts**

  The number of contacts is not limited for use on a logic line. As many NC contacts as required can be connected by means of [OR] [NOT] keys.



Coding

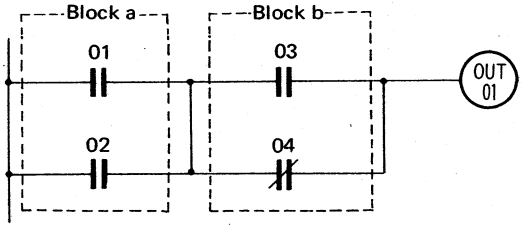
OP	Sub OP	Data
LD		01
OR·NOT		02
OR·NOT		03
⋮		⋮
OUT		01

  In this case, the contact of the first relay number 01 is at the start of each logic line. Therefore, the relay contact must be programmed as "LD01."

- The OR·NOT instruction is a parallel connection instruction and is used when all the contacts to be connected in parallel are NC contacts.

■ AND·LOAD (AND·LD) INSTRUCTION

For inter-block AND operation between two or more blocks, use the AND·LD instruction.



Coding

Address	OP	Sub OP	Data
000	LD		01
001	OR		02
002	LD*		03
003	OR·NOT		04
004	AND·LD**		
005	OUT		01

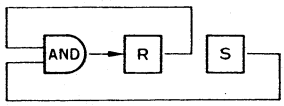
Contents of Registers

R	S
01	—
01 02	—
03	01 02
03 04	01 02
01 03 02 04	—
01 03 02 04	—

NOTES: * Use this instruction as the first instruction for the next block to be ANDed with the preceding block.
** Use the AND·LD instruction for series connection of two blocks (blocks "a" and "b").

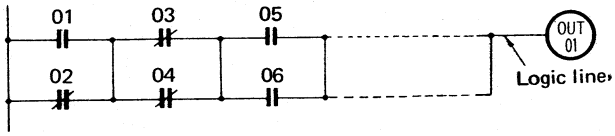
- **Operation of each register**

  1. By the LD01 and OR02 instructions, the result of the logical OR operation in block "a" is stored into the R register.
  2. By the LD03 instruction in block "b", the result of the operation in block "a" is transferred into the S register, while the result of the logical operation by instructions LD03 and OR·NOT04 in block "b" is stored into the R register.
  3. AND·LD instruction causes the logical AND operation to be performed between the R register and the S register. The result of the logical AND operation will be newly stored in the R register.



- **Number of blocks**

  The number of blocks is not limited for AND·LD operation on a logic line. As many blocks as required can be continued for series connection by means of [LD] ~ [AND] [LD] keys.

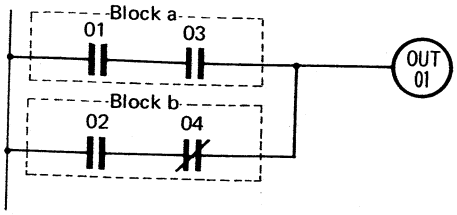


Coding

OP	Sub OP	Data
LD		01
OR·NOT		02
LD·NOT		03
OR·NOT		04
AND·LD		—
LD		05
OR		06
AND·LD		—
⋮		⋮
OUT		01

■ OR-LOAD (OR-LD) INSTRUCTION

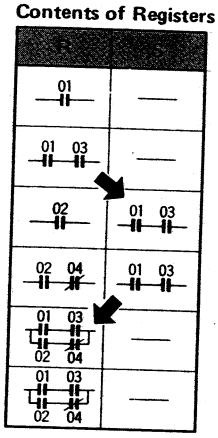
For inter-block OR operation between two or more blocks, use the OR-LOAD instruction.



Coding

Address	OP	Sub OP	Data
000	LD		01
001	AND		03
002	LD*		02
003	AND-NOT		04
004	OR-LD**		
005	OUT		01

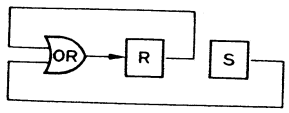
Contents of Registers



NOTES: * Use this LD instruction as the first instruction of the next block to be ORed with the preceding block.
** Use the OR-NOT instruction for parallel connection of two blocks (blocks "a" and "b").

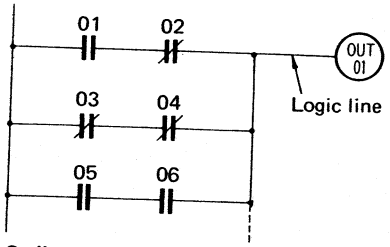
- **Operation of each register**

1. By the LD01 and AND03 instructions, the result of the logicla AND operation in block "a" is stored into the R register.
2. By the LD02 instruction in block "b", the result of the operation in block "a" is transferred into the S register, while the result of the logical operation by instructions LD02 and AND-NOT04 in block "b" is stored into the R register.
3. The OR-LD instruction causes the logical OR operation to be performed between the R register and the S register. The result of the logical OR operation will be newly stored into the R register.



- **Number of blocks**

The number of blocks is not limited for OR-LD operation on a logic line. As many blocks as required can be continued for parallel connection by means of LD ~ OR LD keys.

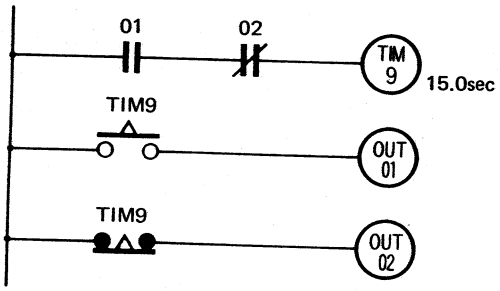


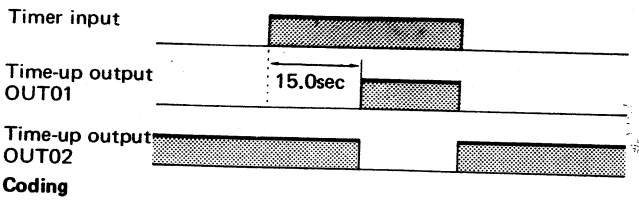
Coding

OP	Sub OP	Data
LD		01
AND-NOT		02
LD-NOT		03
AND-NOT		04
OR-LD		—
LD		05
AND		06
OR-LD		—
⋮		⋮
OUT		01

■ TIMER (TIM) INSTRUCTION

The TIM instruction can be used as an ON-delay timer in the same manner as a relay circuit.



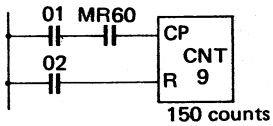


Coding

Address	OP	Sub OP	Data
000	LD		01
001	AND-NOT		02
002	TIM	9*	150**
003	LD	TIM/4	9
004	OUT		01
005	LD-NOT	TIM/4	9
006	OUT		02

NOTES: * Timer number 0 ~ 9.
** Time setting value 001 ~ 255 x 0.1sec

- **Operation of each register**
  The timer starts when the content of the R register is logical 1 and resets when the content of the R register is logical 0.
- **Number of contacts**
  A time-up contact designates the timer number itself. Both NO and NC contacts can be used in the required quantity.
- **Timer is of decrementing type**
  The timer is of a decrementing type which produces an output when the present value (time remaining) becomes "000." When the timer input is turned off, the present value of the timer returns to the preset value. The timer output is transmitted externally through an output relay as shown in the above circuit example.
- **Timer is reset at the time of a power failure**
  If a power failure occurs, the timer is reset and the present value returns to the preset value. Therefore, if it is required to retain the present value of the timer in the memory, a memory retentive type timer circuit as shown below must be used for programming.
- **Memory retentive type timer**
  A circuit to memorize the present value of the timer during a power failure is configured using a combination of clock instruction and counter (CNT) instruction.

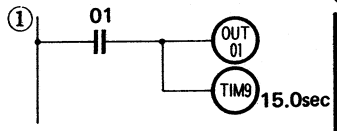


Coding

OP		Data
LD		01
AND	MR/2	60
LD		02
CNT	9	150

NOTE: Timer contact MR60 is for 0.1sec clock. (Use timer contact MR61 for 1sec clock.)

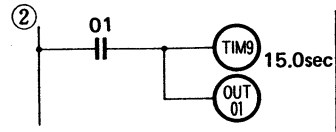
- **Consecutive OUT instruction and TIM instruction**
  If the OUT instruction is followed by the TIM instruction, this condition is regarded as a circuit error during the program check. However, they operate as follows.



Coding

OP		Data
LD		01
OUT		01
TIM	9	150

When the NO contact 01 turns ON, output relay 01 is energized and at the same time timer 9 starts operating.



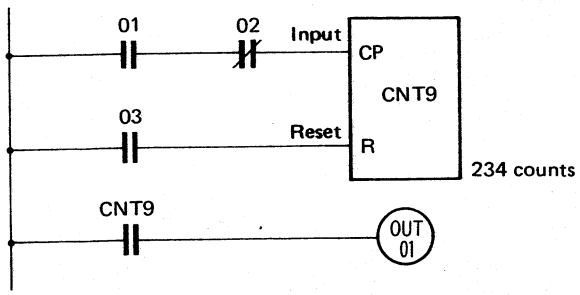
Coding

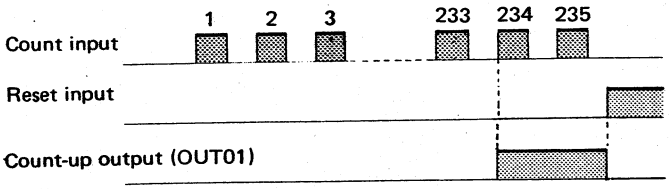
OP		Data
LD		01
TIM	9	150
OUT		01

When the NO contact 01 turns ON, timer 9 starts operating and at the same time, output relay 01 is energized.

■ COUNTER (CNT) INSTRUCTION

The CNT instruction can be used as a preset counter in the same manner as a relay circuit.





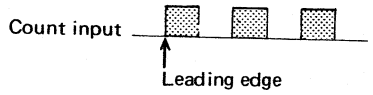
Coding

	OP		
000	LD		01
001	AND-NOT		02
002	LD		03
003	CNT	9*	234**
004	LD	CNT/5	9
005	OUT		01

NOTES:
1. A counter program must be entered in the order of a count input circuit, a reset input circuit and a counter coil.
2. Counter number 0 ~ 9.
3. Counter setting value 001 ~ 255.

- **Operation of each register**
  The counter resets when the content of the R register is logical 1 and is enabled to count when the content of the R register is logical 0. A count input is provided from the S register.
- **Number of contacts**
  A count-up contact designates the counter number itself. Both NO and NC contacts can be used in the required quantity.
- **Counter is of decrementing type**
  The counter is of a decrementing type which produces an output when the count value becomes "000." The present value of the counter returns to the preset value when a reset input is applied. The counter output is transmitted externally through an output relay as shown in the above circuit example.
- After the preset count is up, subsequent count inputs are ignored.

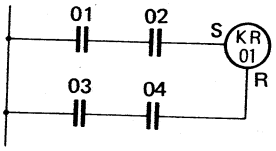
- At the leading edge (i.e., from OFF to ON) of a count input signal, the counter decrements the count value by 1.



- When both a count input and a reset input are applied simultaneously, the reset input takes precedence over the count input. The counter performs counting operation again after the reset input is removed.
- **The present value of the counter is retained in memory during a power failure**
  If a power failure occurs, the counter is not reset and the present value (i.e., count remaining) of the counter is retained in the memory.
  Accordingly, to reset the count value of the counter when power is applied, use the contact of special auxiliary relay MR59 to generate a reset input. (Refer to paragraph 5.2.4, Applied Programs.)

■ LATCHING RELAY (KR) INSTRUCTION

The KR instruction can be used as a latching relay in the same manner as a relay circuit.



Coding

Address	OP	Sub OP	Data
000	LD		01
001	AND		02
002	LD		03
003	AND		04
004	OUT*	KR/3	01

Contents of Registers

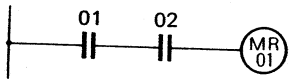
R	S
01	—
01 02	—
03	01 02
03 04	01 02
03 04	01 02

NOTE: * A latching relay program must be entered in the order of a set input circuit, a reset input circuit and a latching relay coil. Use the OUT instruction to program a latching relay coil.

- **Operation of each register**
  The latching relay operates when the content of the R register is logical 0 and the content of the S register is logical 1. The relay releases when the content of the R register is logical 1.
- When both a set input and a reset input are applied simultaneously, the reset input takes precedence over the set input.
- The content of the latching relay is retained in the memory during a power failure. It continues to be retained until application of a reset input.

■ INTERNAL AUXILIARY (MR) INSTRUCTION

This instruction is used when an internal auxiliary relay is employed.



Coding

Address	OP	Sub OP	Data
000	LD		01
001	AND		02
002	OUT*	MR/2	01

Contents of Registers

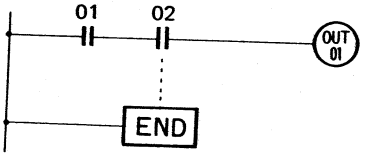
R	S
01	—
01 02	—
01 02	—

NOTE: * The OUT instruction is used to program an internal auxiliary relay coil.

- Internal auxiliary relays have no relation whatsoever to input/output relays. However, the internal auxiliary relay contacts cannot be used as external outputs.
- The number of contacts is not limited for use.

■ END INSTRUCTION

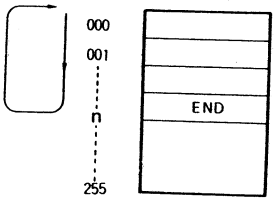
Insert this instruction at the end of a program.



Coding

Address	OP	Sub OP	Data
000	LD		01
001	AND		02
002	OUT		01
003			
004			
⋮	⋮	⋮	⋮
n	END		

- The program memory of the SYSMAC-P0R is provided with addresses 000 to 255. The CPU scans program data from address 000 to address with an END instruction according to the ladder diagram.



- When performing a test run, insert an END instruction at each end of a sequence circuit and then delete the END instruction after confirming each circuit. In this manner, the test run can be executed smoothly.
- When the mode selector switch is set to the RUN mode without an END instruction being inserted at the end of a program, the RUN indicator illuminates. In this case, however, error message " ♀ " appears in the Sub OP code display, and the program cannot be executed.

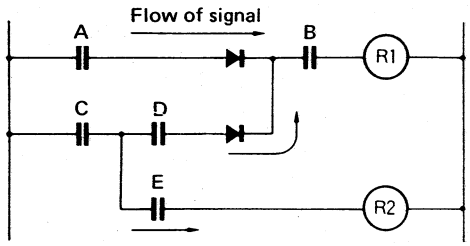
5. Programming

5.1 How to Program

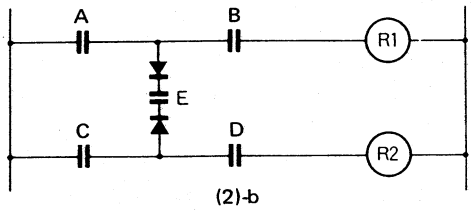
With the SYSMAC-P0R, a ladder circuit is controlled according to the sequence of the instructions stored in the CPU memory. Therefore, it is neccessary to observe the hints on correct programming and programming order.

5.1.1 Hints on correct programming

1. Since the number of contacts is not limited for input/output relays, internal auxiliary relays, timers, etc., it can be said that the best way to design a ladder circuit is to configure a simple, clear circuit, rather than a complicated circuit created by reducing the number of contacts.
2. In the SYSMAC-P0R, signals will flow from the left to the right. In other words, signals will flow as if diodes are inserted in the circuit as shown in (2)-a or (2)-b. To operate a circuit without diodes in the same manner as the circuit configured with general control relays, it is necessary to rewrite the circuit.

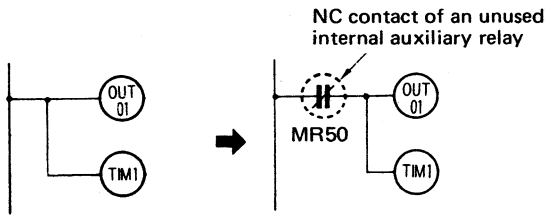


(2)-a

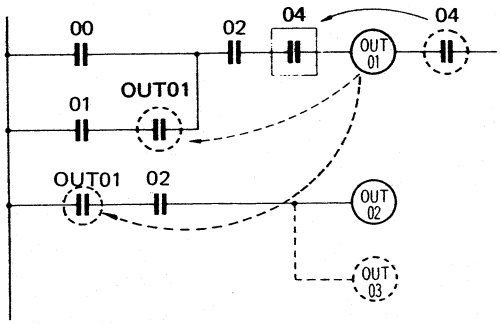


(2)-b

3. In a series-parallel circuit, the number of contacts that can be connected in series is not limited, as well as the number of contacts that can be connected in parallel.
4. No output relay can be connected directly from the bus bar. If necessary, connect it through the NC contact of an unused internal auxiliary relay.



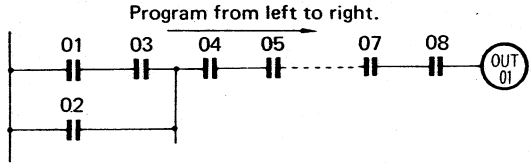
5. All output relays are provided with auxiliary contacts that can be used on a circuit, in addition to the output signal contacts to drive loads actually. The number of contacts that can be used per output relay is not limited.



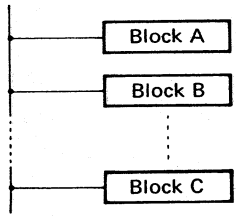
6. No relay contact can be inserted next to an output coil. If necessary, insert it before the output coil.
7. Two or more output coils can be connected in parallel. In this case, however, note that a circuit error message will appear in the display.
8. For contact and coil numbers on the circuit, use the I/O relay numbers described in Chapter 3.
9. Output coil numbers (including those for timers and counters) cannot be used in duplication.

5.1.2 Programming order

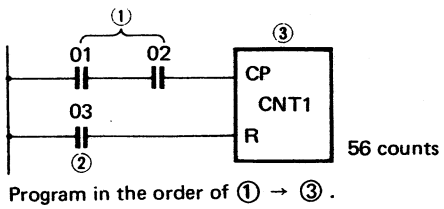
1. Program a circuit from its left to right.



2. Assume the circuit elements located from the bus bar to an output relay as one block. If a number of blocks are in line, programming can be started from any block. However, pay attention in case of circuits utilizing scan time or timing such as differentiator, shift register, etc.



3. When composite instructions such as counter, latching relay, etc. are used, their order of programming is predetermined. Be sure to perform the programming according to the predetermined order.

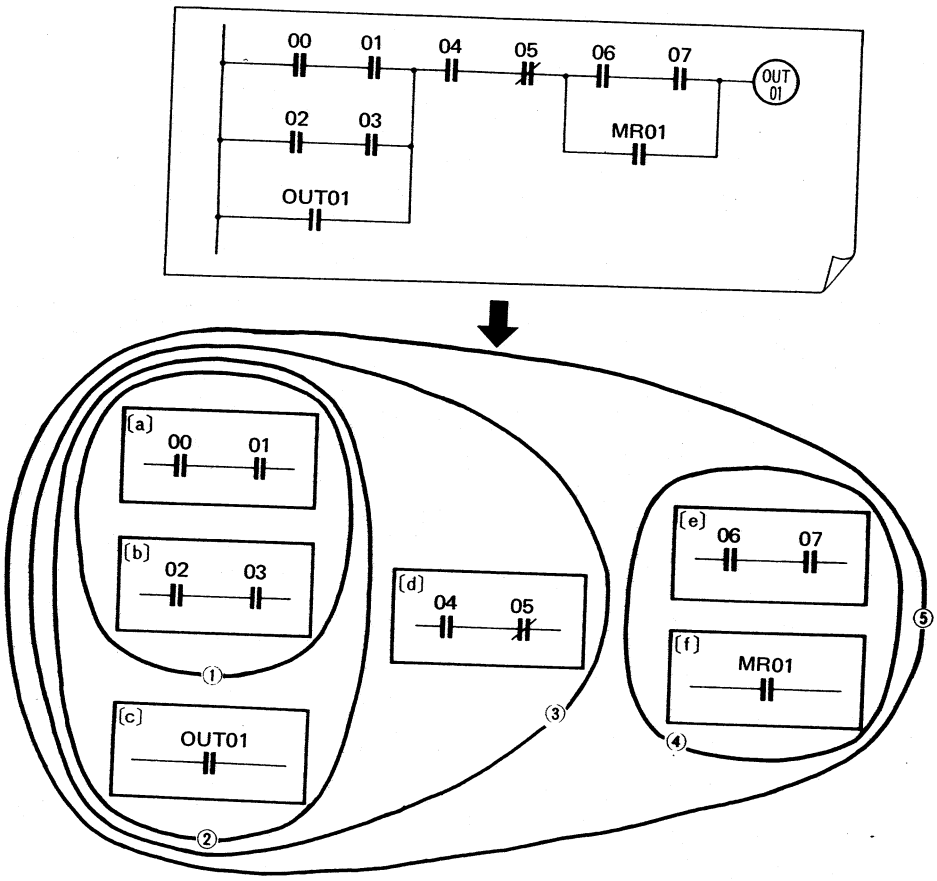


Program in the order of ① → ③.

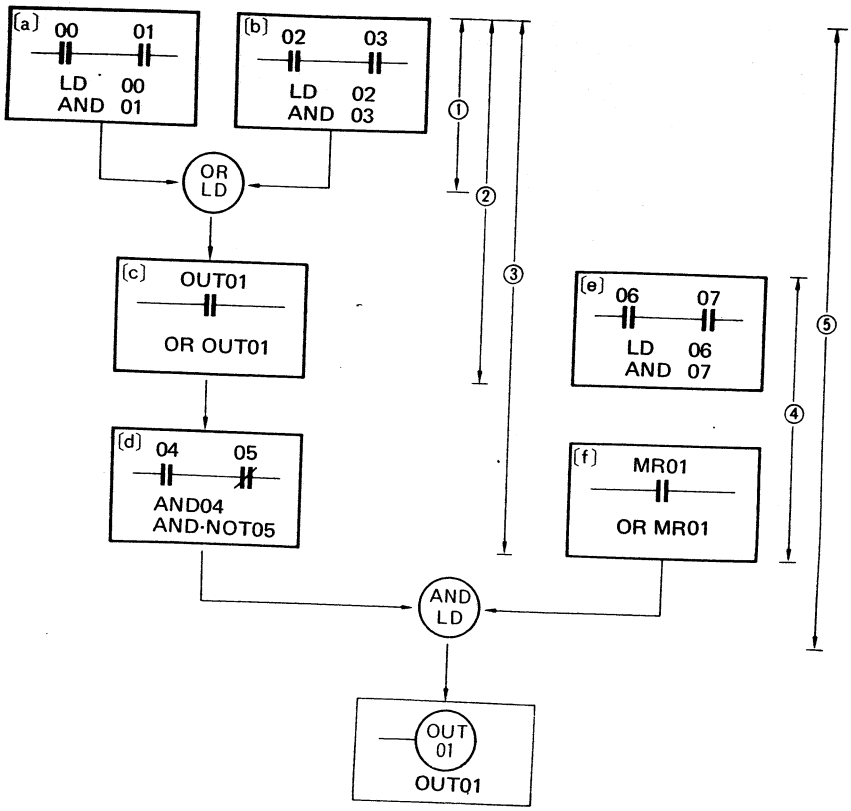
Address	Instruction	Sub-OP	Data
⋮	⋮		⋮
n	LD		01
n + 1	AND		02
n + 2	LD		03
n + 3	CNT	1	56
⋮	⋮	⋮	⋮

4. Be sure to insert an END instruction at the end of each program.
5. A ladder diagram such as the one shown below can be divided into small blocks as shown below, to program each block in the order of ① to ⑤. Eventually, the circuit will be programmed as one large block such as ⑤.

- **Ladder diagram**



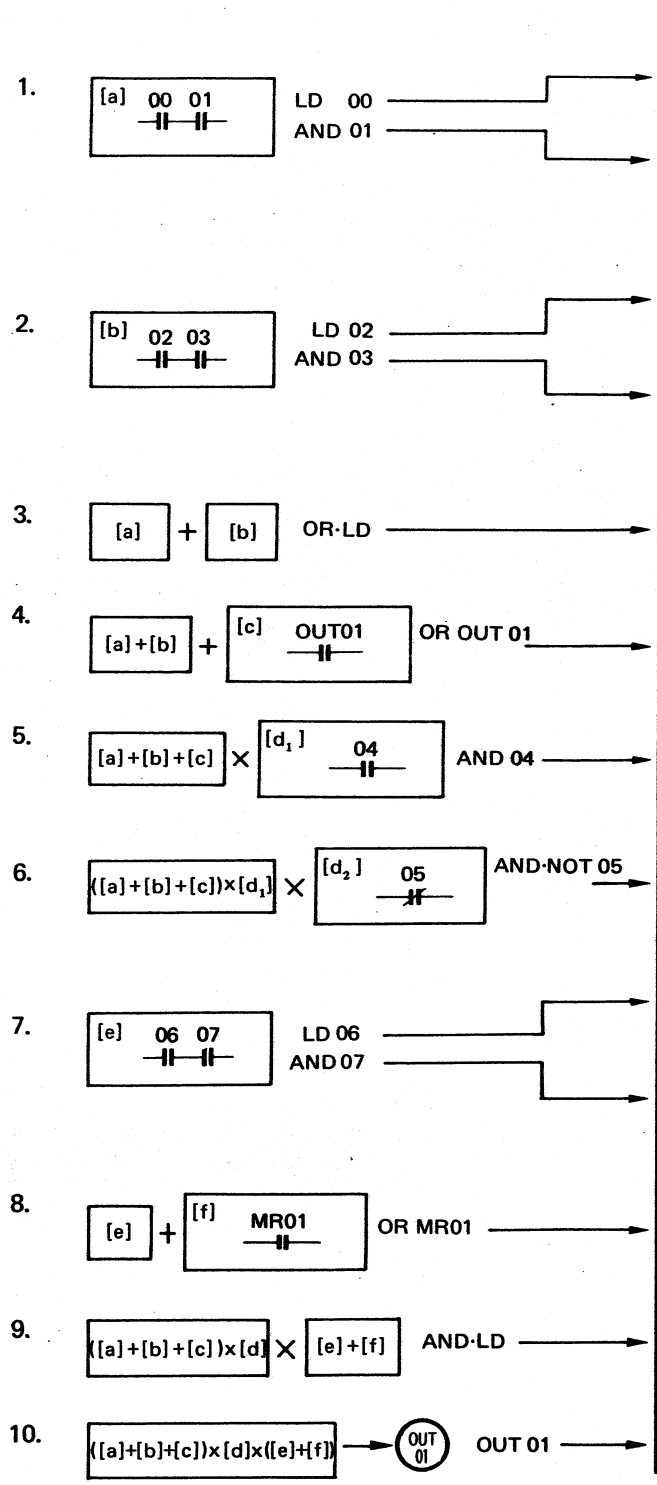
- **Programming procedure**



- **Coding**

Address	OP	Sub OP	Data
000	LD		00
001	AND		01
002	LD		02
003	AND		03
004	OR·LD		
005	OR	OUT/1	01
006	AND		04
007	AND·NOT		05
008	LD		06
009	AND		07
010	OR	MR/2	01
011	AND·LD		
012	OUT		01
⋮	⋮		⋮
n	END		

- **Operations of R and S registers**

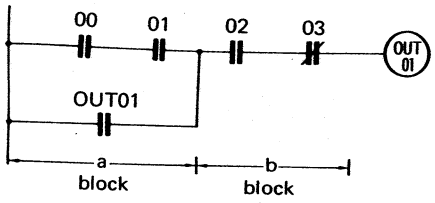


Content of register	R register	S register
The content ("1" or "0") of 00 is stored in R register.	00	Vacant
The content of R register is ANDed with the content of 01 and the result of operation is stored in R register.	Result of 00 01 = [a]	Vacant
The previous content of R register is transferred to S register and the content of 02 is newly stored in R register.	02	[a]
The content of R register is ANDed with the content of 03, and the result of operation is stored in R register.	Result of 02 03 = [b]	[a]
The content of R register (result [b]) is ORed with the content of S register (result [a]), and the result of operation is stored in R register.	Result of ORing [a] with [b] = [a]+[b]	Vacant
The content of OUT 01 is ORed with the content of R register, and the result of operation is stored in R register.	Result of ORing [a]+[b] with [c] = [a]+[b]+[c]	Vacant
The content of 04 is ANDed with the content of R register, and the result of operation is stored in R register.	Result of ANDing [a]+[b]+[c] with $[d_1]$ = [a]+[b]+[c] x$[d_1]$	Vacant
The content of 05 is ANDed with the content of R register and the result of operation is stored in R register.	Result of ANDing [a]+[b]+[c] x$[d_1]$ with $[d_2]$ = ([a]+[b]+[c]) +$[d_2]$	Vacant
The previous content of R register is transferred to S register, and the content of 06 is stored in R register.	06	[a] [b] [c] [d]
The content of R register is ANDed with the content of 07, and the result of operation is stored in R register.	Result of 06 07 = [e]	[a] [b] [c] [d]
The content of R register is ORed with the content of MR01, and the result of operation is stored in R register.	Result of ORing [e] with [f] = [e]+[f]	[a] [b] [c] [d]
The content of R register is ANDed with the content of S register, and the result of operation is stored in R register.	([a]+[b]+[c]) x[d]x[e]+[f]	Vacant
The result of R register is output to output relay OUT01.	([a]+[b]+[c]) x[d]x([e]+[f])	Vacant

5.2 Applied Programs

5.2.1 When LD/OR/AND/NOT instructions are used

1. An example of parallel-series circuit

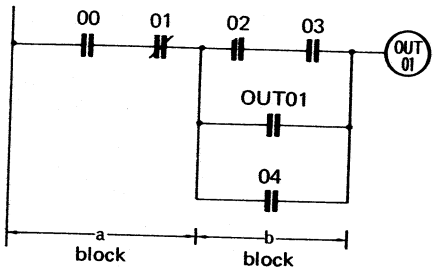


Coding

OP	Sub OP	Data	
LD		00	a
AND		01	
OR	OUT/1	01	
AND		02	b
AND-NOT		03	
OUT		01	
⋮	⋮	⋮	
END			

- Process block "b" after programming block "a" (parallel circuit).
- For coding, enter I/O relay numbers in the data field.

2. An example of series-parallel circuit

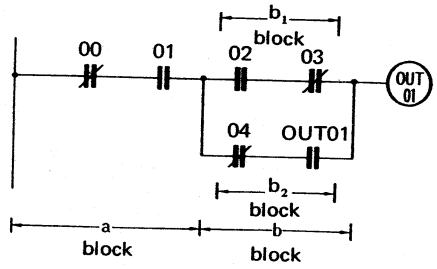


Coding

OP	Sub OP	Data	
LD		00	a
AND-NOT		01	
LD		02	b
AND		03	
OR	OUT/1	01	
OR		04	
AND-LD			
OUT		01	
⋮	⋮	⋮	
END			

- Divide the circuit into blocks "a" and "b" and program each block.
- Then combine blocks "a" and "b" by AND-LD instruction.

3. An example of series-parallel circuit

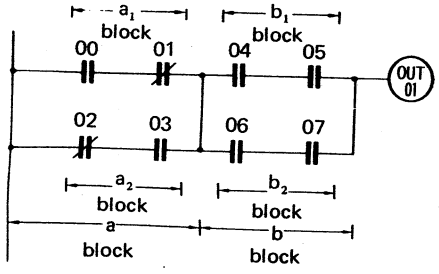


Coding

OP	Sub OP	Data	
LD-NOT		00	a
AND		01	
LD		02	b_1
AND-NOT		03	
LD-NOT		04	b_2
AND	OUT/1	01	
OR-LD			b_1+b_2
AND-LD			a·b
OUT		01	
⋮	⋮	⋮	
END			

- Program block "a".
- Program block "b_1" and then block "b_2".
- Combine blocks "b_1" and "b_2" using OR-LD instruction.
- Combine blocks "a" and "b" using AND-LD instruction.

4. An example of connecting parallel circuits in series

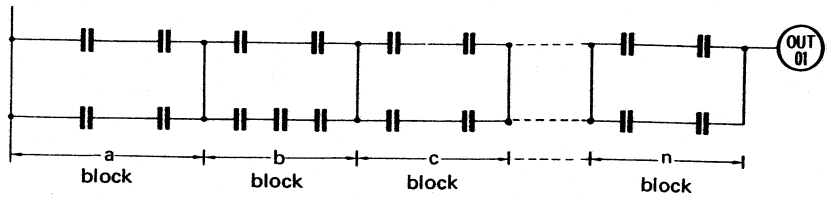


Coding

OP	Sub OP	Data	
LD		00	a_1
AND-NOT		01	
LD-NOT		02	a_2
AND		03	
OR-LD			a_1+a_2
LD		04	b_1
AND		05	
LD		06	b_2
AND		07	
OR-LD			b_1+b_2
AND-LD			a·b
OUT		01	
⋮	⋮	⋮	
END			

- Program block "a_1" and then block "a_2" and combine both blocks using OR-LD instruction.
- Program blocks "b_1" and "b_2" in the same manner as above.
- Combine blocks "a" and "b" using AND-LD instruction.

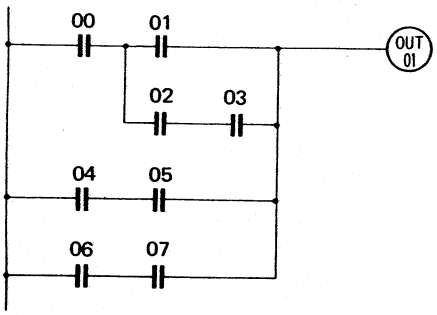
5. An example of connecting parallel circuits in series



- When a number of blocks continue from block number "a" to "n," the programming procedure is the same as paragraph 4 above. Namely, program the circuit the following sequence.

① block a → ② block b → ③ blocks a·b → ④ block c → ⑤ blocks a·b·c → ⑥ · · · ·

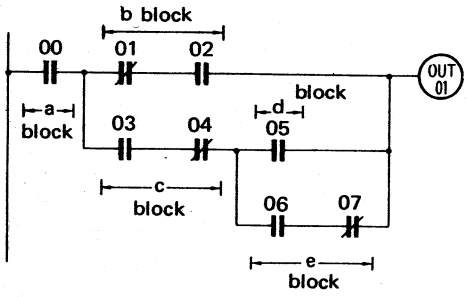
6. An example of complicated parallel circuit



Coding

OP	Sub OP	Data
LD		00
LD		01
LD		02
AND		03
OR·LD		
AND·LD		
LD		04
AND		05
OR·LD		
LD		06
AND		07
OR·LD		
OUT		01
⋮	⋮	⋮
END		

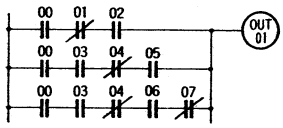
7. An example of complicated circuit



Coding

OP	Sub OP	Data	
LD		00	a
LD·NOT		01	b
AND		02	
LD		03	c
AND·NOT		04	
LD		05	d
LD		06	e
AND·NOT		07	
OR·LD			d+e
AND·LD			(d+e)·c
OR·LD			(d+e)·c+b
AND·LD			[(d+e)·c+b]·a
OUT		01	
⋮	⋮	⋮	
END			

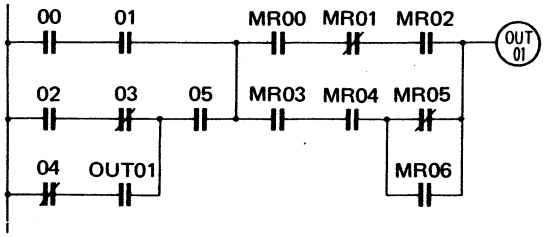
- The circuit shown on the left may be rewritten as follows.



Coding

LD		00
AND·NOT		01
AND		02
LD		00
AND		03
AND·NOT		04
AND		05
OR·LD		
LD		00
AND		03
AND·NOT		04
AND		06
AND·NOT		07
OR·LD		
OUT		01
⋮	⋮	⋮
END		

8. An example of complicated circuit

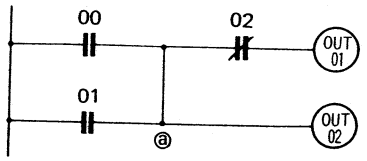


Coding

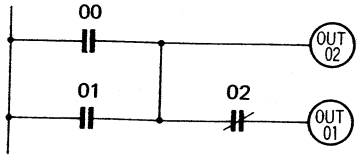
LD		00
AND		01
LD		02
AND·NOT		03
LD·NOT		04
AND	OUT/1	01
OR·LD		
AND		05
OR·LD		
LD	MR/2	00
AND·NOT	MR/2	01

AND	MR/2	02
LD	MR/2	03
AND	MR/2	04
LD·NOT	MR/2	05
OR	MR/2	06
AND·LD		
OR·LD		
AND·LD		
OUT		01
⋮	⋮	⋮
END		

9. An example of circuit requiring caution

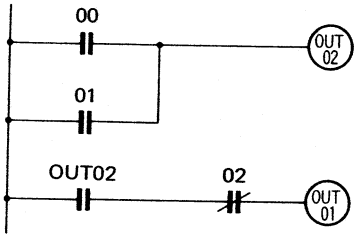


- In such a case as shown above, program relay contact 02 after programming output relay OUT02. This action is necessary for the following reason. Even if an output is sent to OUT02, the content of the R register at point @ will remain unchanged. However, if 02 is programmed before OUT02, the content of the R register at point @ will change and differ from the content sent to OUT02.



- In the case of the above circuit diagram, the circuit operation is possible, but note that this circuit configuration is regarded as a program error during the program check.

or



* This circuit configuration is not regarded as a program error.

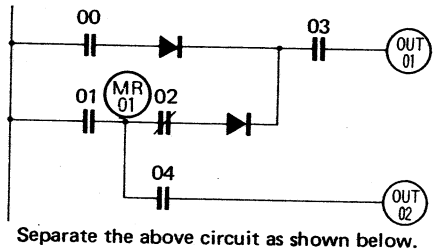
Coding

OP	Sub OP	Data
LD		00
OR		01
OUT		02
AND-NOT		02
OUT		01
⋮	⋮	⋮
END		

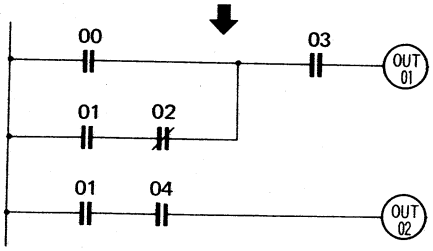
Coding

OP	Sub OP	Data
LD		00
OR		01
OUT		02
LD	OUT/1	02
AND-NOT		02
OUT		01
⋮	⋮	⋮
END		

10. An example of circuit requiring caution



- Separate the above circuit as shown below.



Coding

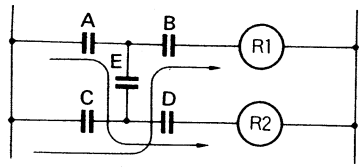
OP	Sub OP	Data
LD		00
LD		01
AND-NOT		02
OR-LD		
AND		03
OUT		01
LD		01
AND		04
OUT		02
⋮	⋮	⋮
END		

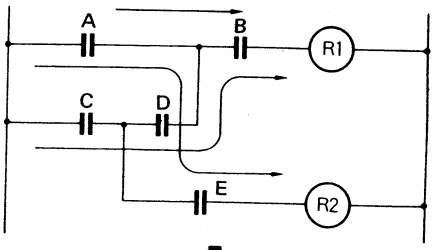
- If the circuit is to be programmed without separating it, program an unused internal auxiliary relay after relay contact 01 The following table shows an example of programming MR 01 after 01

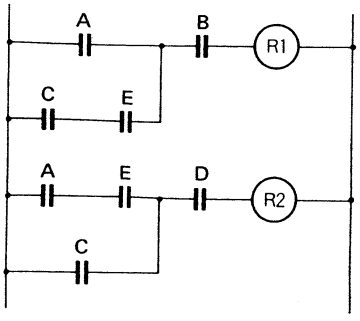
Coding

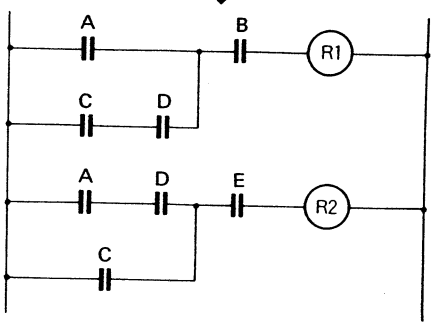
OP	Sub OP	Data
LD		00
LD		01
OUT	MR/2	01
AND-NOT		02
OR-LD		
AND		03
OUT		01
LD	MR/2	01
AND		04
OUT		02
⋮	⋮	⋮
END		

11. Examples of circuit requiring rewrite







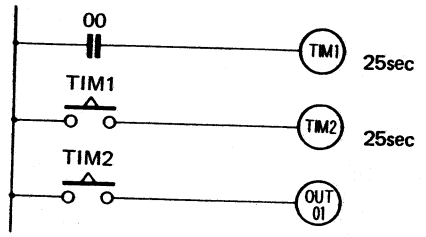


- Such circuits as the two upper circuits shown on the left cannot be programmed and must therefore be rewritten as shown directly below.
- Since the two upper circuits are respectively configured with control relays, the circuits operate even by the flows of signals shown by the arrows. To permit the similar circuit operation with the SYSMAC-P0R, the two upper circuits must be rewritten into the corresponding circuits shown below.

5.2.2 When TIM/CNT instructions are used

1. Long-time timer (25.5sec or more)

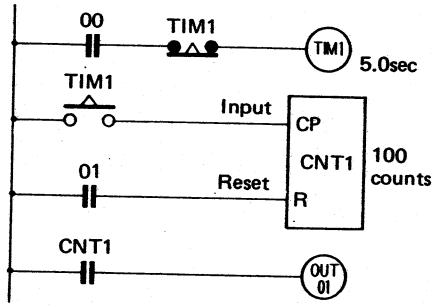
a. Series connection of TIM instructions



Coding

OP	Sub OP	Data
LD		00
TIM	1	250
LD	TIM/4	1
TIM	2	250
LD	TIM/4	2
OUT		01
⋮	⋮	⋮
END		

b. Use of CNT instruction

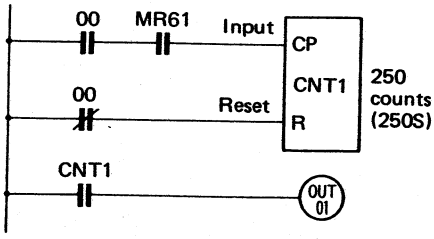


Coding

OP	Sub OP	Data
LD		00
AND-NOT	TIM/4	1
TIM	1	050
LD	TIM/4	1
LD		01
CNT	1	100
LD	CNT/5	1
OUT		01
⋮	⋮	⋮
END		

- In this circuit, a pulse is generated every 5 seconds by timer TIM1 and then pulses at intervals of 5 seconds are counted by counter CNT1. The example shown here is a 500 sec timer. The setting time of the timer is (timer + scan time) x number of counts.
- The present count value of the counter is retained in memory even if the power switch of the SYSMAC-P0R is turned off.

c. Use of internal clock pulse

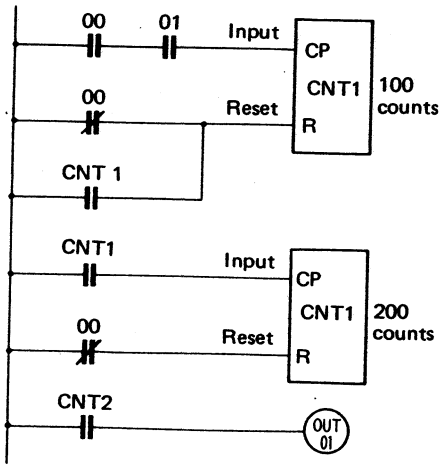


Coding

OP	Sub OP	Data
LD		00
AND	MR/2	61
LD-NOT		00
CNT	1	250
LD	CNT/5	1
OUT		01
⋮	⋮	⋮
END		

- The SYSMAC-P0R has two internal clock pulses (1.0sec pulse: MR61, 0.1sec pulse: MR60). By counting either of the pulses with a counter, a long-time timer can be developed.
- As CNT instruction is employed, the present count value is retained in memory even after the power is turned off.

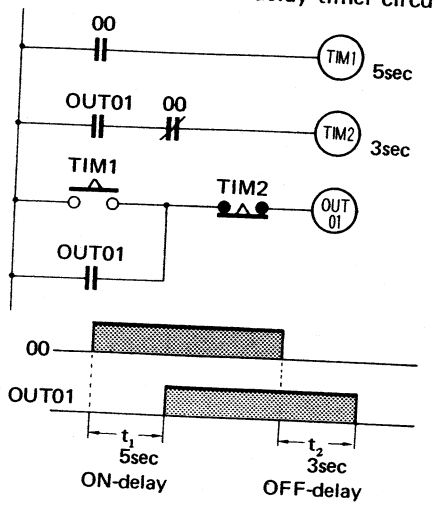
2. Multi-digit counter (255 counts or more)
e.g., 20,000 counts



Coding

OP	Sub OP	Data
LD		00
AND		01
LD-NOT		00
OR	CNT/5	1
CNT	1	100
LD	CNT/5	1
LD-NOT		00
CNT	2	200
LD	CNT/5	2
OUT		01
⋮	⋮	⋮
END		

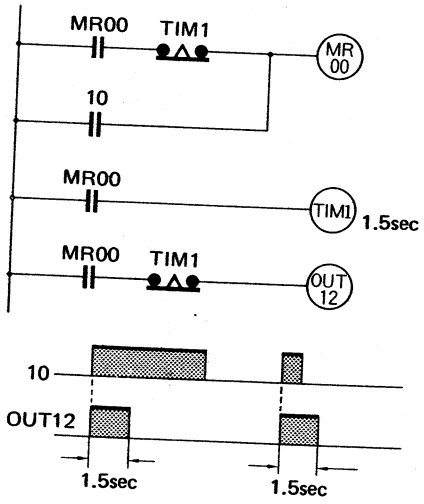
3. An example of ON/OFF-delay timer circuit



Coding

OP	Sub OP	Data
LD		00
TIM	1	050
LD	OUT/1	01
AND-NOT		00
TIM	2	030
LD	TIM/4	1
OR	OUT/1	01
AND-NOT	TIM/4	2
OUT		01
⋮	⋮	⋮
END		

4. An example of one shot timer circuit



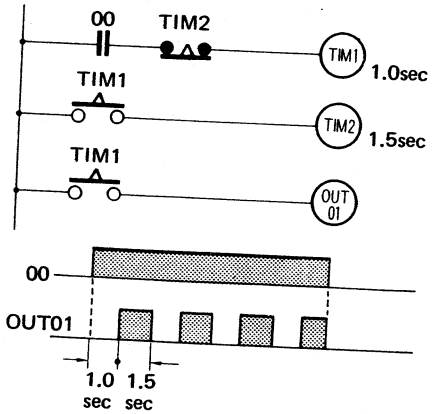
Coding

OP	Sub OP	Data
LD	MR/2	00
AND-NOT	TIM/4	1
OR		10
OUT	MR/2	00
LD	MR/2	00
TIM	1	015
LD	MR/2	00
AND-NOT	TIM/4	1
OUT		12
⋮	⋮	⋮
END		

- One shot output is produced for only the set time of TIM1 after an input signal is applied.

5. Examples of flicker circuit

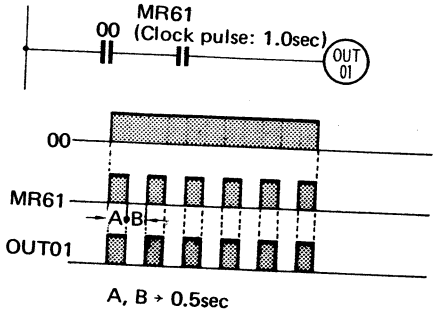
a. With 2 timers used



Coding

OP	Sub OP	Data
LD		00
AND-NOT	TIM/4	2
TIM	1	010
LD	TIM/4	1
TIM	2	015
LD	TIM/4	1
OUT		01
⋮	⋮	⋮
END		

b. With clock pulses



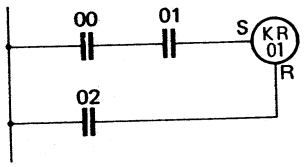
Coding

OP	Sub OP	Data
LD		00
AND	MR/2	61
OUT		01
⋮	⋮	⋮
END		

- Using an internal clock pulse (0.1sec or 1.0sec), a flicker circuit can be processed easily. In this case, however, the flickering time is available only in the following 2 types.
  Special auxiliary relay number MR61: 1.0sec clock pulse
  Special auxiliary relay number MR60: 0.1sec clock pulse

5.2.3 When latching relay is used

1. Basic circuit

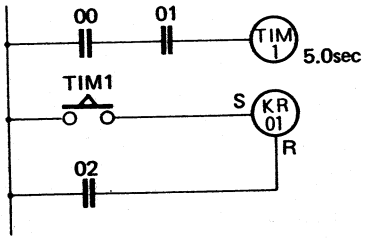


Coding

OP	Sub OP	Data
LD		00
AND		01
LD		02
OUT	KR/3	01
⋮	⋮	⋮
END		

- In the event of a power failure, the ON/OFF state before power failure can be retained in memory, using a latching relay. SYSMAC-P0R has 47 latching relays with relay numbers KR00 ~ KR46.
- Memory retention time after a power failure is about 2 years just the same as that of the program memory.

2. A circuit to keep the time-up state

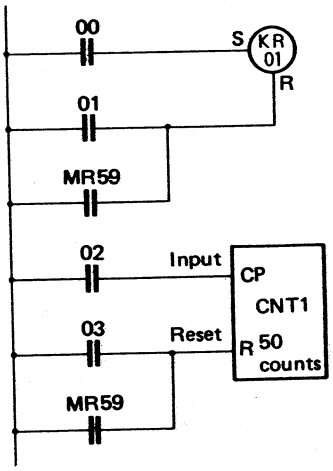


Coding

OP	Sub OP	Data
LD		00
AND		01
TIM	1	050
LD	TIM/4	1
LD		02
OUT	KR/3	01
⋮	⋮	⋮
END		

5.2.4 When Special Auxiliary Relay MR59 is used

1. A circuit to initialize a counter and a latching relay when power is applied



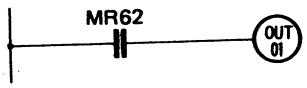
Coding

OP	Sub OP	Data
LD		00
LD		01
OR	MR/2	59
OUT	KR/3	01
LD		02
LD		03
OR	MR/2	59
CNT	1	050
⋮	⋮	⋮
END		

- Special auxiliary relay MR59 is turned on for 1 scan time when power is applied in the RUN mode or when the mode selector switch is changed from "STOP" to "RUN" position.

5.2.5 When Special Auxiliary Relay MR62 is used

1. A circuit to transmit a battery fault signal to an output terminal



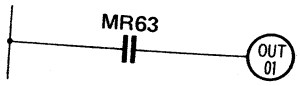
Coding

OP	Sub OP	Data
LD	MR/2	62
OUT		01
⋮	⋮	⋮
END		

- Relay MR62 is turned on when the battery voltage drops or when the battery voltage drops or when the battery is not loaded.
- If a buzzer is connected to the terminal of output relay OUT01, MR62 can be used to issue alarm.
- When the battery is restored to normal, MR62 is turned off.

5.2.6 When Special Auxiliary Relay MR63 is used

1. A circuit to transmit a memory fault signal to an output terminal



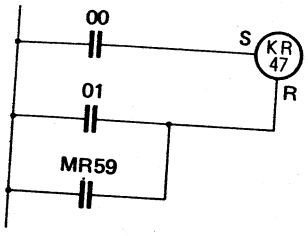
Coding

OP	Sub OP	Number
LD	MR/2	63
OUT		01
⋮	⋮	⋮
END		

- Special auxiliary relay MR63 is turned on when a memory failure occurs and the ERROR indicator flashes on and off.
- MR63 is turned off when a power failure occurs or when the mode selector switch position is changed.
- If a buzzer is connected to the terminal of OUT01, MR63 can be used to issue alarm.

5.2.7 When Special Latching Relay KR47 is used

1. A circuit to inhibit all outputs



Coding

OP	Sub OP	Number
LD		00
LD		01
OR	MR/2	59
OUT	KR/3	47
⋮	⋮	⋮
END		

- When special latching relay KR47 is turned on, all outputs are inhibited, causing all output relays to release. At this time, all the OUTPUT indicators go out and the RUN indicator flashes on and off.
- When special latching relay KR47 is turned off, all the outputs are released from the inhibited state.

6. Operating Procedure

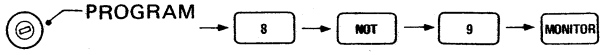
6.1 Basic Functions

Items of Operation	Description
All program clear	Since the CPU retains previously stored data in memory (by battery back-up), all the memory contents must be cleared to write a new program into the memory.
Address setting	Address setting is required to designate an address in such operations as program read, program write, etc.
Program write	This operation is to store a program in the specified memory address.
Program read	This operation is to confirm whether or not data has been programmed properly in the specified memory address.
Program check	This operation is to confirm whether or not the program data written into the CPU memory through the program console are in agreement with the predetermined rules (syntax).
RUN	This operation is to place the SYSMAC-P0R in the RUN (Program Execution) state.
Monitor	This operation is to display the operating state of each relay, or the present value of each timer or counter during the execution of a program.
Trace (continuity) check	When a circuit operation is to be checked in a program simulation or test run, this operation allows the operating state of each relay number to be displayed while tracing the programming sequence of the circuit.
Instruction search	When a circuit change is to be made in a program simulation or test run, this operation allows an address where an instruction has been written in a program to be searched.
Contact (coil) number change	This operation is to change the contact (or coil) number in a program due to a circuit modification.
Contact (coil) addition	This operation is employed when the contact (or coil) number is to be added due to a circuit modification.
Contact (coil) deletion	This operation is to delete the contact (or coil) number from a program due to a circuit modification.
EPROM write	This operation is to transfer the contents of the RAM to the specified EPROM bank.
EPROM read	This operation is to transfer the contents of the specified EPROM bank to the RAM.
EPROM verify	This operation is to verify the contents of the specified EPROM bank against the contents of the RAM.
Tape write	This operation is to record the contents of the RAM (program memory) on a cassette tape.
Tape read	This operation is to transfer the program data recorded on the cassette tape into the RAM.
Tape verify	This operation is to verify the contents of the RAM against the programmed data recorded on a cassette tape.

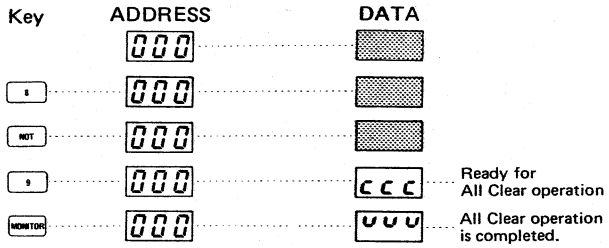
6.2 All Program Clear Operation

Since the CPU retains previously stored data in memory (by battery back-up), all the memory contents must be cleared to write a new program into the memory.

- **Operating procedure**



- **Display**



NOTES:

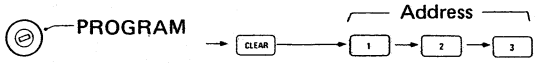
1. By the All Clear operation, all the programs (I/O relays, internal auxiliary relays, latching relays, timers and counters) stored in addresses 000 ~ 255 are cleared.
2. Before the key operation, change the mode selector switch position from other mode to "PROGRAM."
3. In the All Clear operation, a beep sound is generated at the depression of each key.

CAUTION:
After the PROGRAM mode selection, depression of CLEAR key or any key other than the four keys shown above will not allow All Clear operation to be executed. In this case, repeat the operation starting from the mode selection. For example, if the PROGRAM mode was originally changed from the RUN mode, do not set the mode selector to the RUN mode again. First set it to the STOP mode and then to the PROGRAM mode to repeat the operation.

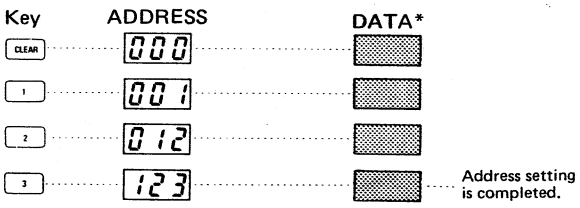
6.3 Address Setting Operation

Address setting is required to designate an address in such operations as program read, program write.

- **Operating procedure**

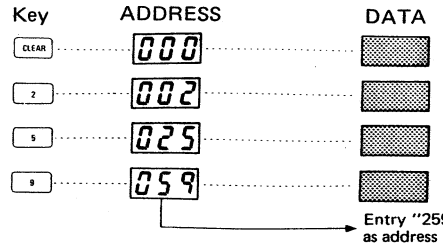


- **Display**



NOTES:

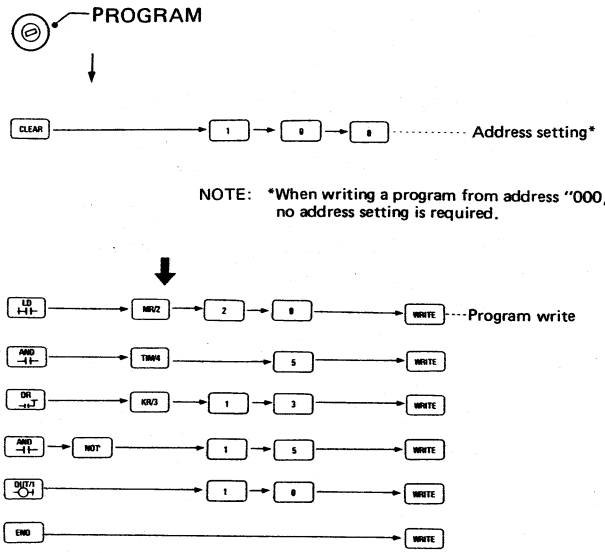
1. Each address is set in 3 digits using numeric 000 ~ 255. To set address "000," no numeric entry is required. To set address "003," depress only numeric key 3 and to set address "023," depress only numeric keys 2 and 3. Preceding zero(es) may be omitted from key entry.
2. * The data entered will not be displayed by the address setting operation alone. To display the data entered, [*] [,] keys must be depressed.
3. In address setting, when numeric data entered as an address exceeds 255, the first digit of the 3-digit address is automatically processed as "0." Since the CPU does not recognize this as an error, the only way to identify this error is through confirmation by the operator.
   For example, if address 259 is entered, it will be set as follows.



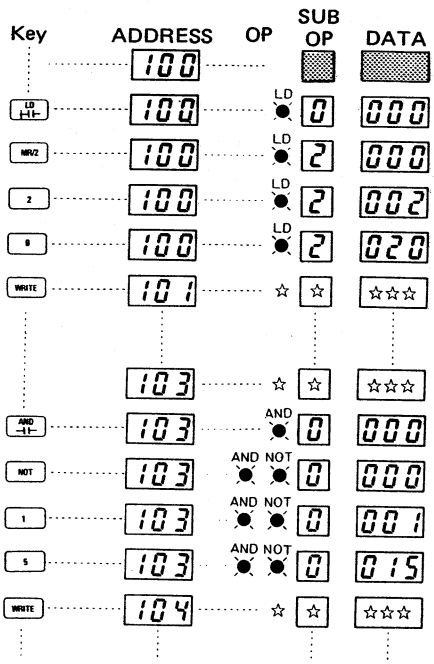
6.4 Program Write Operation

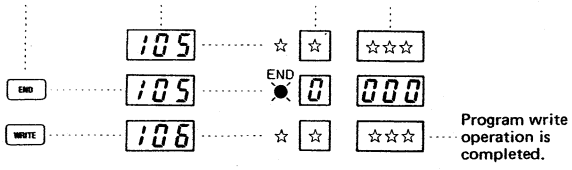
This operation is to store a program in the specified memory address.

- **Operating procedure**

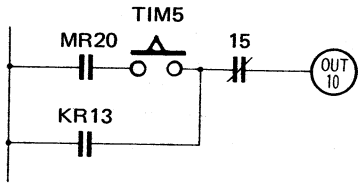


- **Display**





- **Circuit for exercise and programming example**



Coding

Address	OP	Sub OP	DATA
100	LD	MR/2	20
101	AND	TIM/4	5
102	OR	KR/3	13
103	AND-NOT		15
104	OUT		10
105	END		
106	⋮	⋮	⋮

NOTES:

1. In the left-hand figure, ☆☆☆ indicates that the content of the memory at the displayed address will appear in the DATA display. Accordingly, after the All Clear operation, nothing will appear in the OP display and zeroes will appear in the SUB OP and DATA displays, respectively.
2. Depression of the **WRITE** key causes the contents appearing in the OP, SUB OP and DATA displays to be stored into the memory address specified by the ADDRESS display and at the same time causes the memory address to be incremented by one.

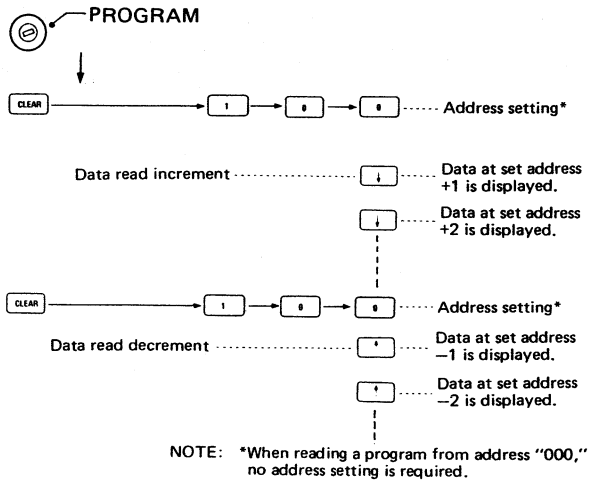
Correction Procedures when an error occurs in program write

1. If an error in programming is noticed before depressing the WRITE key, depress the CLEAR DISPLAY key and the re-entry operation from OP code becomes effective.
2. If an error is programming is discovered after depressing the WRITE key, repeat the operation from the address setting, or return to the address in which the error exists by depressing the ↑ key and then depress the CLEAR DISPLAY key and the re-entry operation from OP code becomes effective.

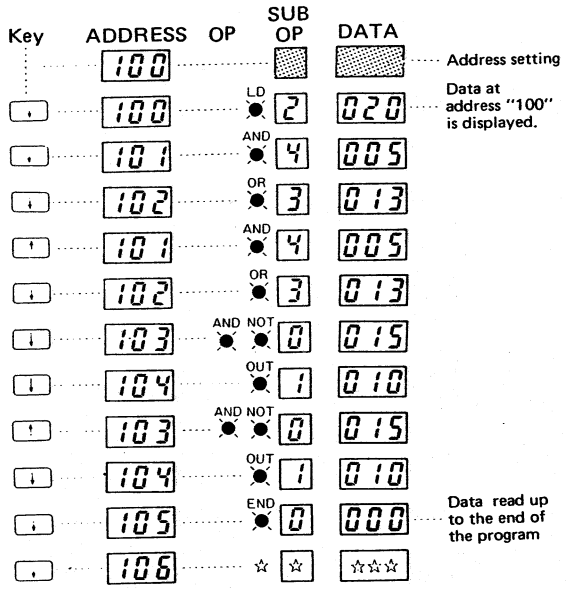
6.5 Program Read Operation

This operation is to confirm whether or not the data has been programmed properly in the specified memory address.

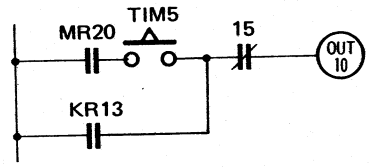
- **Operating procedure**



- **Display**



- **Circuit for exercise and programming example**



Coding

Address	OP	Sub OP	Data
100	LD	MR/2	20
101	AND	TIM/4	5
102	OR	KR/3	13
103	AND·NOT		15
104	OUT		10
105	END		
106	⋮		⋮

NOTES:
1. At each depression of the [↓] key, the data at the set address +1 is displayed (i.e., data read increment).
2. At each depression of the [↑] key, the data at the set address −1 is displayed (i.e., data read decrement).

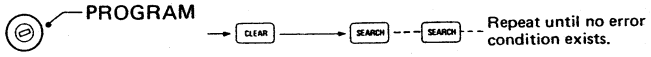
6.6 Program Check Operation

This operation is to confirm whether or not the program data written into the CPU memory through the program console are in agreement with the predetermined rules (syntax).

Items subject to program check are as follows.

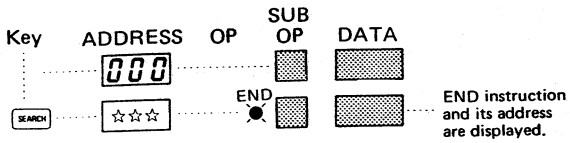
- Coil duplication error
- Circuit error
- END instruction missing error

- **Operating procedure**

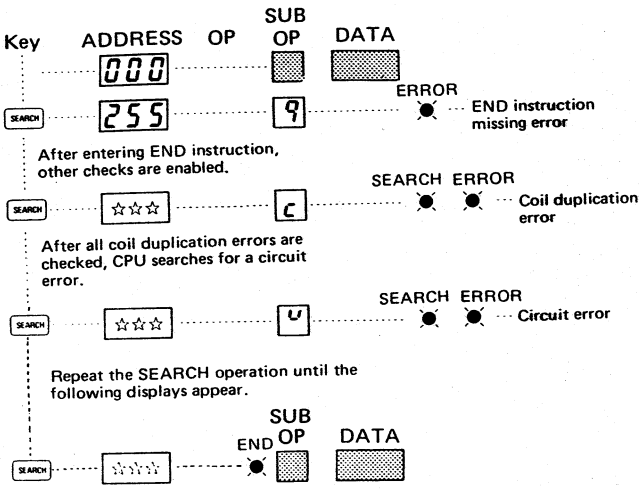


- **Display**

When a program error does not exist



When a program error exists



- **Error conditions**

1. END instruction missing error
   In the absence of an END instruction at the last address of a program, error message " 9 " appears in the SUB OP display. If this error occurs, the CPU cannot perform other item checks. After entering an END instruction, the CPU is enabled to perform other item checks.
2. Coil duplication error
   If a program contains OUT, OUT MR/2, OUT KR/3, TIM or CNT instructions of the same number, error message " C " appears in the SUB OP display. After all the coil duplication errors have been checked, the CPU performs circuit error check.
3. Circuit error
   This check is intended to manage the R and S registers. As a method, the difference between the number of logical start instructions (LD, LD·NOT, etc.) and the number of inter-block logic instructions (AND·LD, OR·LD) is computed, and if the difference is abnormal when the results of the operation (OUT, OUT MR/2, OUT KR/3, TIM and CNT) are executed, this condition is regarded as a circuit error.

NOTES:
1. Priority in program check is as follows: END instruction missing error > coil duplication error > circuit error.
2. If any programming error is discovered, correct the erroneous program in accordance with the program write procedure.

6.7 RUN Operation

This operation is to place the SYSMAC-P0R in the RUN (Program Execution) condition.

- **Operating procedure**

NOTES:

1. In the RUN mode, sum check, watchdog timer check and battery check are automatically performed. If any error occurs in the respective checks, the status indicators and the state of program execution by CPU become as shown below. (See paragraph 8.5, Troubleshooting for details.)

	ERROR indicator	RUN indicator	BAT monitor	State of program execution by CPU
Sum check	●	◐		Continues
Watchdog timer	●	○		Stops
Battery failure		◐	●	Continues

○ mark indicates the indicator goes out.
● mark indicates the indicator lights.
◐ mark indicates the indicator flashes ON and OFF.

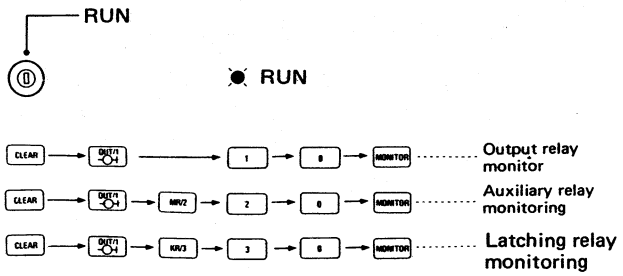
2. In other than the RUN mode, all external outputs are turned off. When the mode selector switch position is changed from "STOP" to "RUN," the SYSMAC-P0R is placed in the same state when power is applied.

6.8 Monitor Operation

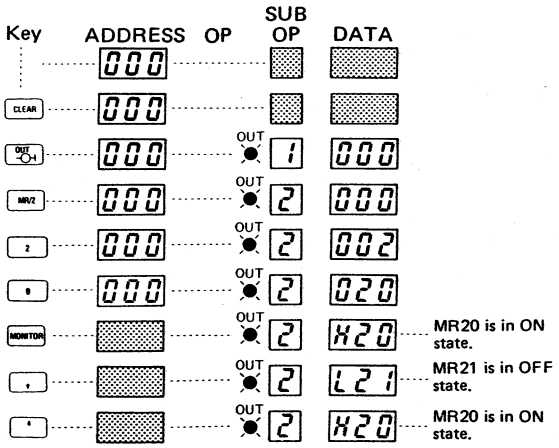
This operation is to display the operating state of each relay, or the present value of each timer or counter during the execution of a program.

■ MONITORING OF THE OPERATING STATE OF AN OUTPUT RELAY, INTERNAL AUXILIARY RELAY OR LATCHING RELAY

- **Operating procedure**

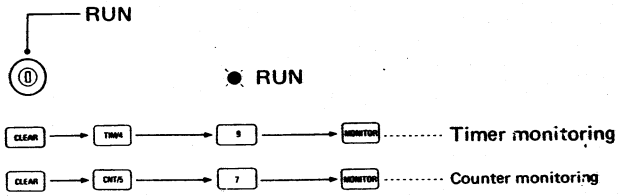


- **Display**

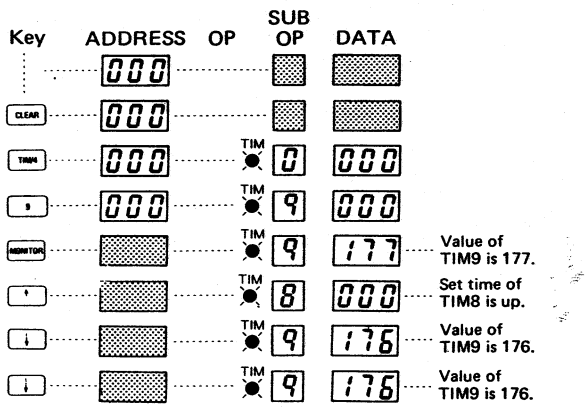


■ MONITORING OF THE CURRENT VALUE OF A TIMER, OR COUNTER

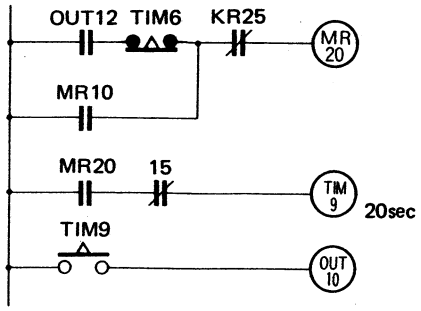
- **Operating procedure**



- **Display**



- **Circuit for exercise and programming example**



Coding

Address	OP	Sub OP	Data
100	LD	OUT/1	12
101	AND-NOT	TIM/4	6
102	OR	MR/2	10
103	AND-NOT	KR/3	25
104	OUT	MR/2	20
105	LD	MR/2	20
106	AND-NOT		15
107	TIM	9	200
108	LD	TIM/4	9
109	OUT		10
110	END		

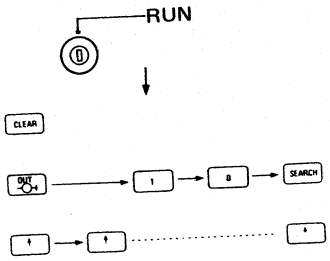
NOTES:
1. As the operating state of each output relay, auxiliary relay, or latching relay, "H" or "L" is displayed at the MSD position of the DATA display.
   "H" (High level) is displayed when the state of the set relay number is ON.
   "L" (Low level) is displayed when the state of the set relay number is OFF.
2. As the present value of each timer or counter, 3-digit data is displayed in the ADDRESS display. When the set time of the set timer number is up (or the set value of the set counter number is counted out), "000" will appear in the 3-digit positions of the DATA display.
3. At each depression of the [↑] or [↓] key following the MONITOR key, the relay number, timer number or counter number is incremented or decremented respectively by 1. Thus, the state of each relay, timer, or counter can be monitored in succession.

6.9 Trace (Continuity) Check Operation

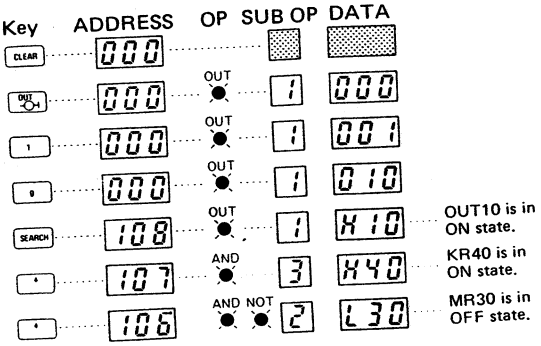
When a circuit operation is to be checked in a program simulation or test run, this operation allows the operating state of each relay number to be displayed while tracing the programming sequence of the circuit.

- **Operating procedure**

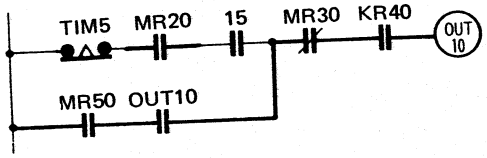
  In the circuit for exercise shown on the right, the procedure to check the operating states of respective relays from (OUT 10) to —TIM5— in the programming sequence is shown below.



- **Display**



- **Circuit for exercise and programming example**



Coding

Address	OP	Sub OP	Data
100	LD-NOT	TIM/4	5
101	AND	MR/2	20
102	AND		15
103	LD	MR/2	50
104	AND	OUT/1	10
105	OR-LD		
106	AND-NOT	MR/2	30
107	AND	KR/3	40
108	OUT		10
109	END		
110			

NOTES:
1. The following two methods of trace check are available.
   - Check starting from address 000

     CLEAR → [↑] → [↑] ····· [↑]
   - Check starting from an OUT instruction (OUT, OUT MR/2, OUT KR/3, TIM, or CNT).

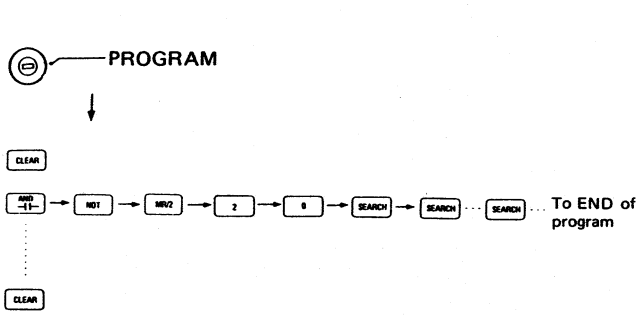
     CLEAR → OUT → MR/2 → 5 → 0 → SEARCH → [↑] → [↑]
2. In the RUN mode, the SEARCH operation is possible for OUT, OUT MR/2, OUT KR/3, TIM and CNT instructions only.
3. In the RUN mode, a beep sound is generated when the output instruction has been searched.
4. When the relay number represented by the low-order 2 digits of the DATA display is in the ON state, "H" will appear in the MSD position of the DATA display. When the relay number is in the OFF state, "L" will appear in the MSD position of the DATA display. This indicates the ON/OFF state of the relay number without relation to the presence or absence of a NOT instruction. In other words, if "L" appears when a NOT instruction is entered, it indicates that the relay is in the energized state.
5. Search of timer or counter.
   When a timer or counter is searched in the RUN mode, the present value of the timer or counter is not displayed. "H" is displayed when the set time (or set count) is up, while "L" is displayed when the set time (or set count) is remaining.

6.10 Instruction Search Operation

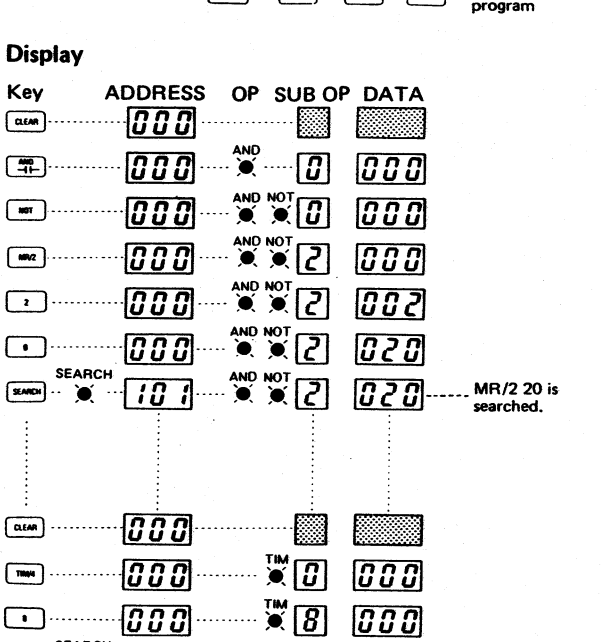
When a circuit change is to be made in a program simulation or test run, this operation allows an address where an instruction has been written in a program to be searched.

- **Operating procedure**

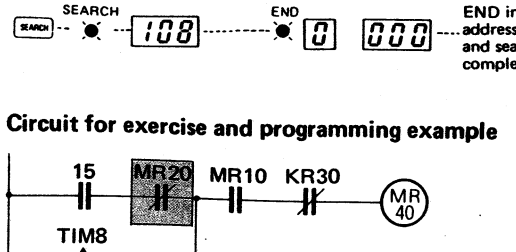
  Referring to the circuit for exercise and programming example shown below, an example of searching MR02 and (TIM 8) instructions is explained here.



- **Display**



- **Circuit for exercise and programming example**



shows the instruction to be searched.

Coding

Address	OP	Sub OP	Data
100	LD		15
101	AND-NOT	MR/2	20
102	OR	TIM/4	8
103	AND	MR/2	10
104	AND-NOT	KR/3	30
105	OUT	MR/2	40
106	LD	MR/2	50
107	TIM	8	105
108	END		
109			
110			

NOTES:

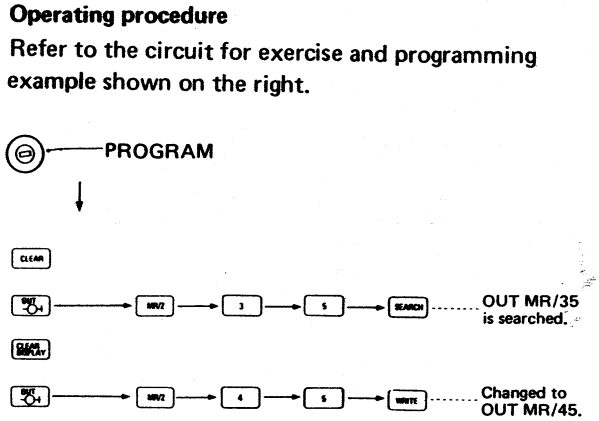
1. When the SEARCH key is depressed after entering an instruction, the first address where the instruction is stored is displayed. Continued depression of the SEARCH key causes all the addresses containing this instruction to be searched until the END instruction is encountered.
2. If the program has no END instruction, the CPU cannot perform the search operation. This condition is indicated as "END instruction missing error" on the SUB OP display and the ERROR indicator will be illuminated if such a condition occurs.
3. If the instruction entered is not contained in the program, depression of the SEARCH key causes the END address to be displayed.
4. When a TIM or CNT instruction is to be searched, it is unnecessary to enter the setting value of the timer or counter.
5. A search operation is completed when the CLEAR or CLEAR DISPLAY key is depressed or after the search of an END instruction in a program. Upon completion of the search operation, the SEARCH indicator will go out.

6.11 Contact (Coil) Number Change Operation

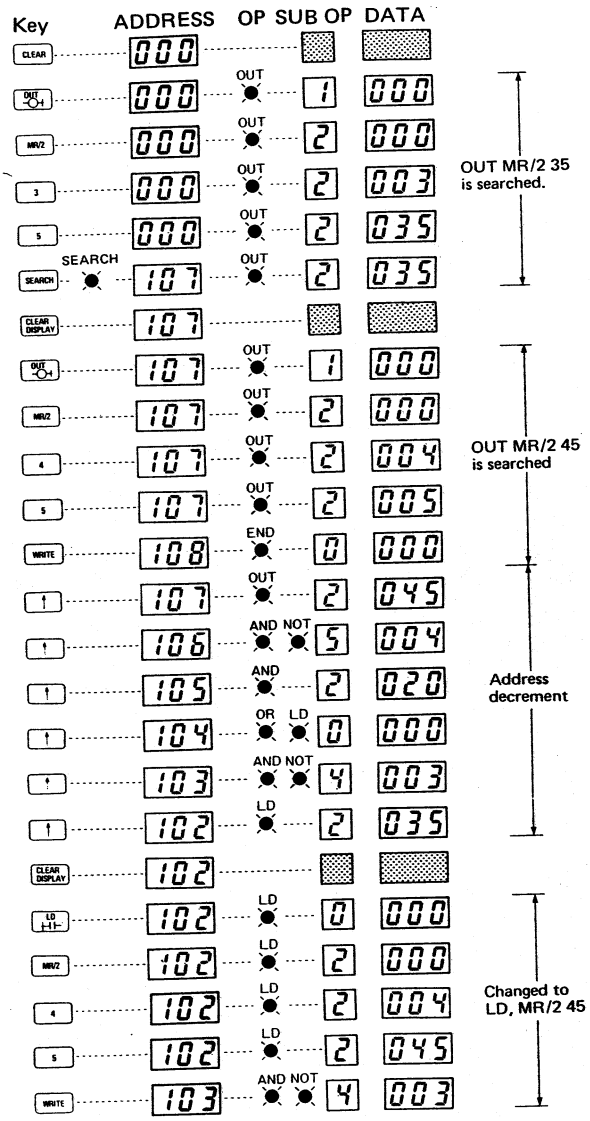
This operation is to change the contact (or coil) number in a program due to a circuit modification.

- **Operating procedure**

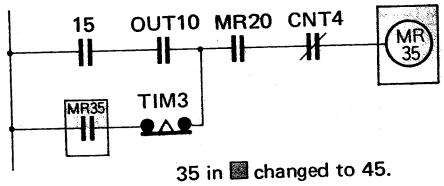
  Refer to the circuit for exercise and programming example shown on the right.



- **Display**



- **Circuit for exercise and programming example**



35 in ■ changed to 45.

Coding

Address	OP	Sub OP	Data
100	LD		15
101	AND	OUT/1	10
102	LD	MR/2	35
103	AND-NOT	TIM/4	3
104	OR-LD		
105	AND	MR/2	20
106	AND-NOT	CNT/5	4
107	OUT	MR/2	35
108	END		
109			
110			

NOTES:

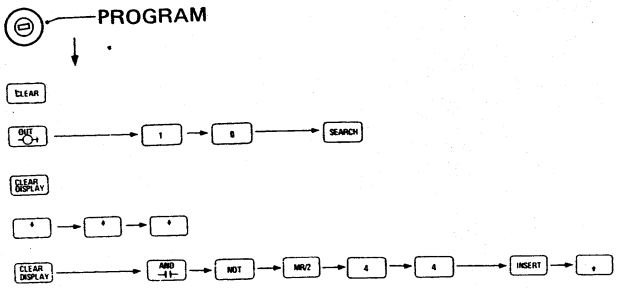
1. After an OUT instruction has been searched, depress the [↑] or [↓] key continuously to decrement the address number until the address where the contact (coil) number is to be changed. The instruction to be changed at an intended address may be searched directly. However, the same instruction may in some cases be stored in other memory addresses of the same program. Therefore, it is necessary to check instructions before and after the intended address. Since no two OUT instructions with an identical relay number exist in one program, the instruction to be changed can be found easily and quickly by first searching the OUT instruction and then searching before and after the OUT instruction.
2. When the contact (coil) number of an OUT, TIM, or CNT instruction is to be changed, confirm the circuit related to the instruction.
3. After the contact (coil) number has been changed, be sure to perform the Program Check operation ([CLEAR] → [SEARCH]) to confirm that the program is free from any programming error.

6.12 Contact (Coil) Addition Operation

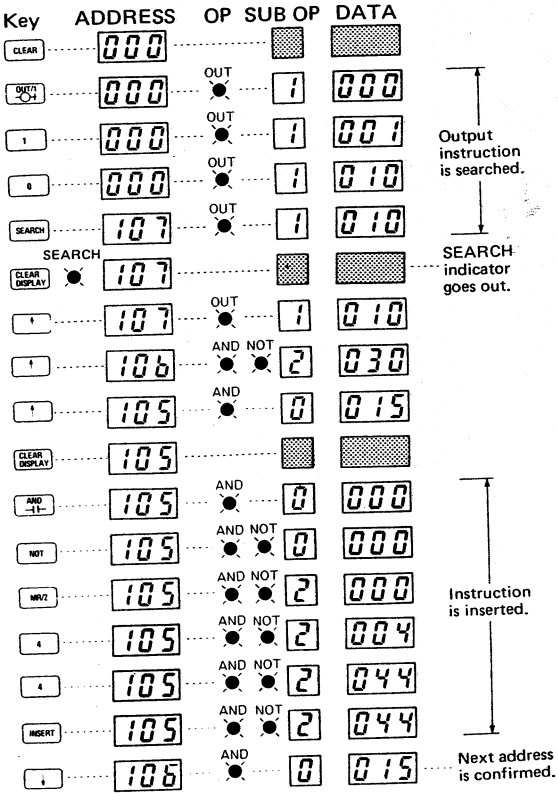
This operation is employed when the contact (or coil) number is to be added due to a circuit modification.

- **Operating procedure**

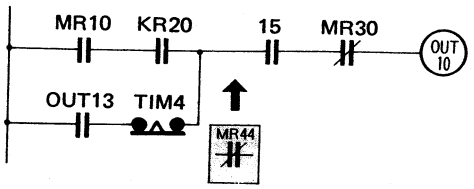
In the following, the procedure of adding MR44 ⊣⊢ before 15 ⊣⊢ is shown.



- **Display**



- **Circuit for exercise and programming example**



Coding

Address	OP	Sub OP	Data
100	LD	MR/2	10
101	AND	KR/3	20
102	LD	OUT/1	13
103	AND-NOT	TIM/4	4
104	OR-LD		
105	AND		15
106	AND-NOT	MR/2	30
107	OUT		10
108	END		
109			
110			

Coding

Address	OP	Sub OP	Data
100	LD	MR/2	10
101	AND	KR/3	20
102	LD	OUT/1	13
103	AND-NOT	TIM/4	4
104	OR-LD		
105	AND-NOT	MR/2	44
106	AND		15
107	AND-NOT	MR/2	30
108	OUT		10
109	END		
110			

NOTES:

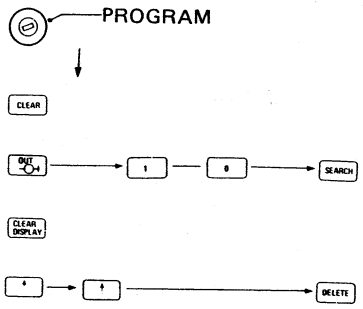
1. When an instruction entered for addition is in excess of the program capacity, the INSERT key input will not be accepted and thus the instruction cannot be inserted.
2. After the instruction to be inserted has been entered, depression of the INSERT key two or more times in succession will be ignored and no instruction can be entered.
3. After the insertion of the instruction, confirm instructions before and after the inserted address.
4. After the contact (coil) has been inserted, be sure to perform the Program Check operation (CLEAR → SEARCH) to confirm that the program is free from any programming error.

6.13 Contact (Coil) Deletion Operation

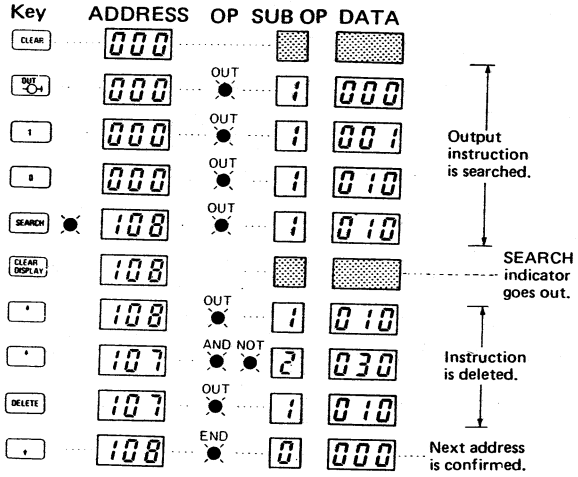
This operation is to delete the contact (or coil) number from a program due to a circuit modification.

- **Operating procedure**

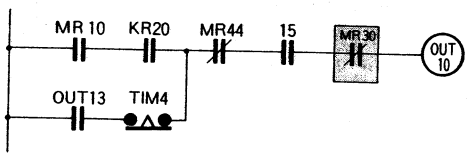
  Referring to the circuit for exercise shown below, an example of deleting MR30 is explained.



- **Display**



- **Circuit for exercise and programming example**



☐ indicates the instruction to be deleted.

Coding

Address	OP	Sub OP	Data
100	LD	MR/2	10
101	AND	KR/3	20
102	LD	OUT/1	13
103	AND-NOT	TIM/4	4
104	OR-LD		
105	AND-NOT	MR/2	44
106	AND		15
107	AND-NOT	MR/2	30
108	OUT		10
109	END		
110			

Coding

Address	OP	Search	Data
100	LD	MR/2	10
101	AND	KR/3	20
102	LD	OUT/1	13
103	AND-NOT	TIM/4	4
104	OR-LD		
105	AND-NOT	MR/2	44
106	AND		15
107	OUT		10
108	END		
109			
110			

NOTES:
1. After the instruction has been deleted, confirm instructions before and after the deleted address.
2. After the deletion of the instruction, be sure to execute the Program Check operation ([CLEAR]→[SEARCH]). Particularly, the program check is mandatory when such an instruction as LD, OUT, TIM, or CNT is deleted.
3. Note that each depression of the DELETE key causes each instruction being displayed to be deleted successively.

6.14 EPROM Handling

The Type SCYP0R-CPU20 is an EPROM self-contained type CPU. Since the CPU executes programs by reading the contents of the RAM, this type of CPU permits data read, write and verify operations between the RAM and the EPROM when various programs are in use, or for program storage.

■ AVAILABLE TYPE OF EPROM

Type ROM-F (equivalent to 2716)

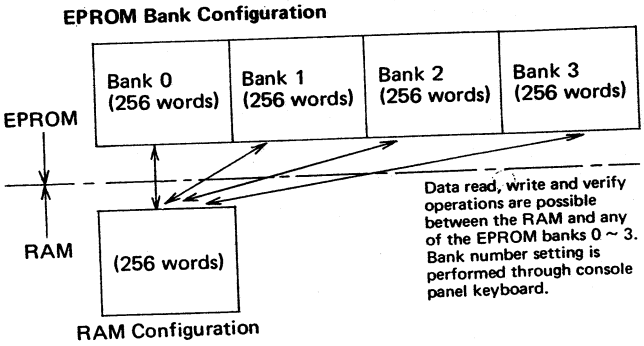
■ MEMORY CAPACITY

4 kinds of user programs (256 RAM addresses x 4) can be stored per EPROM chip.

■ ADDRESS SETTING

The EPROM address area is divided into 4 which are referred to as Bank 0, 1, 2 and 3, respectively. The capacity of one RAM corresponds to one EPROM bank (i.e., 256 words).

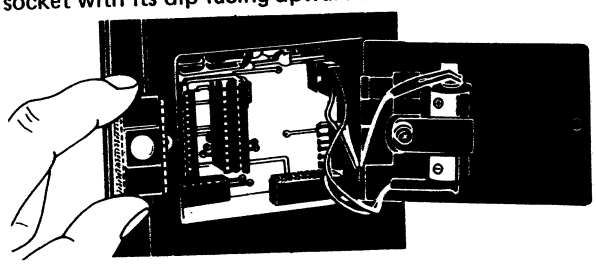
EPROM Bank Configuration



RAM Configuration

■ MOUNTING EPROM CHIP

Be sure to insert the EPROM chip onto the EPROM socket with its dip facing upwards.

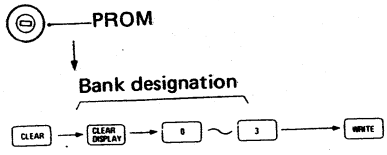


NOTES:
1. Completely erase the EPROM and then write data into the EPROM. The contents of the EPROM are erased by irradiating ultraviolet rays on the EPROM surface through the erase window. The EPROM cannot be erased completely if the irradiation of ultraviolet rays is insufficient. Therefore, be sure to observe the specified erase time. Whether or not the EPROM has been erased completely can be confirmed by the EPROM Verify operation. (Refer to paragraph 6.18, Errors in PROM Mode.)
2. Erase time
   Completely erase the EPROM according to the specifications of the eraser to be used.
3. Frequency of re-programming
   Limit the frequency of re-programming the EPROM to 7 times. If the EPROM is reprogrammed more than 7 times, the EPROM may malfunction.
4. Program protection
   To sustain the reliability of the EPROM, place the EPROM in a protective case or wrap it in aluminum foil if it is not to be used for an extended period.
5. Handling EPROM
   The EPROM is susceptible to static electricity being carried in the human body. When handling the EPROM, avoid touching its pins as much as possible.
6. Removal of EPROM
   The EPROM can be inserted or removed while power is being applied to the SYSMAC-P0R. However, never remove the EPROM chip during the EPROM write, read, or verify operation.
7. After the program debugging, be sure to attach a light-shielding seal to the erase window in order to maintain the reliability of the EPROM chip.

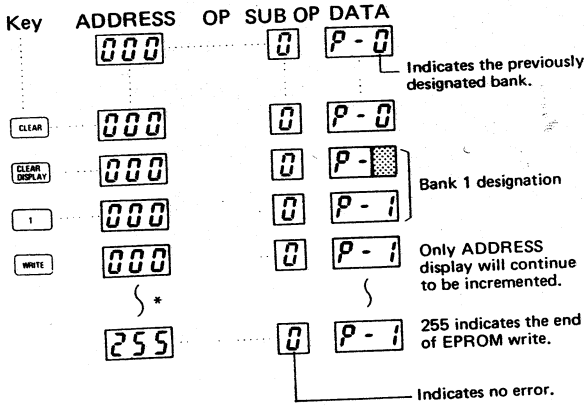
6.15 EPROM Write Operation

This operation is to transfer the contents of the RAM to the specified EPROM bank.

- **Operating procedure**



- **Display**



NOTES:
1. Bank designation is not required if the same bank as that previously set is to be used. Therefore, the only required key operation in this case is as follows.

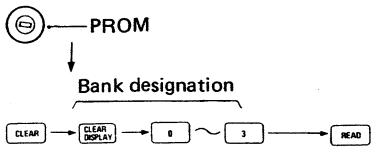
   [CLEAR] → [WRITE]

2. * Upon depression of the WRITE key, only the ADDRESS display will continue to be incremented. When the display shows 255, it indicates that the EPROM write operation has been completed.
3. During the EPROM write operation, if the power is turned off, or the EPROM chip is removed, the EPROM write will be interrupted. In such a case, retry the EPROM write operation from the beginning after erasing the EPROM chip, or use other EPROM.
4. During the EPROM write operation, no PROGRAM key input will be accepted.

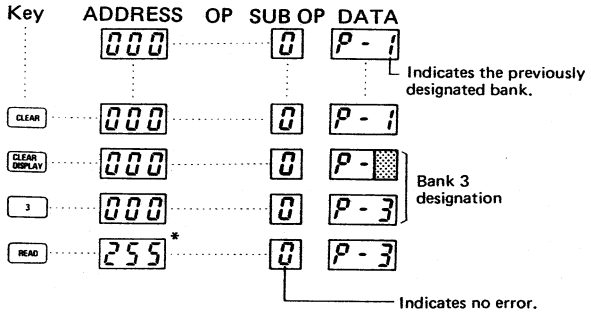
6.16 EPROM Read Operation

This operation is to transfer the contents of the specified EPROM bank to the RAM.

- **Operating procedure**



- **Display**



NOTES:

1. Bank designation is not required if the same bank as that previously set is to be used. Therefore, the only required key operation in this case is as follows.

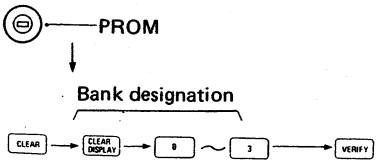
   CLEAR → READ

2. * Upon depression of the READ key, the ADDRESS display shows "255," indicating that the EPROM read operation has been completed (instantaneously) up to address 255.
3. During the EPROM Read operation, if the power is turned off or the EPROM chip is removed, the EPROM read will be interrupted. In such a case, retry the operation from the beginning.

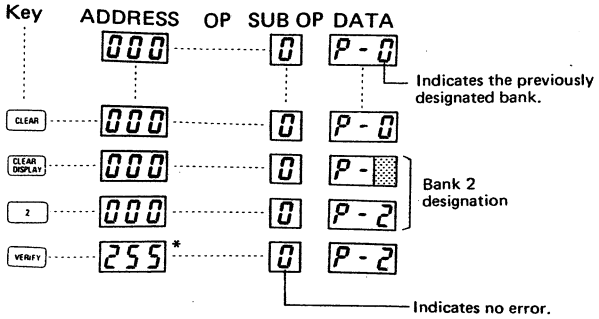
6.17 EPROM Verify Operation

This operation is to verify the contents of the specified EPROM bank against the contents of the RAM.

- **Operating procedure**



- **Display**



NOTES:

1. Bank designation is not required if the same bank as that previously set is to be used. Therefore, the only required key operation in this case is as follows.

   CLEAR → VERIFY

2. * When the contents of the specified EPROM bank agree with the contents of the RAM, the ADDRESS display shows 255, indicating that the EPROM verify operation has been completed (instantaneously) up to address 255.
3. During the EPROM Verify operation, if the power is turned off, or EPROM is removed, the EPROM Verify operation will be interrupted. In such a case, retry the operation from the beginning.

6.18 Errors in PROM Mode

During an EPROM Write, Read or Verify operation, one of the following error messages may appear on the SUB OP display when the ERROR indicator illuminates. The description of each message is as follows.

Operation	Error message	Description
EPROM Write	7	• EPROM is not inserted. • EPROM is inserted with its dip facing downward. • EPROM is inserted but its specified bank has not been erased.
EPROM Read	7	• Nothing has been written into the specified bank of the inserted EPROM.
	8	• EPROM is not inserted.
EPROM Verify	6	• The contents of the specified EPROM bank do not agree with the contents of the RAM.
	7	• Nothing has been written into the specified EPROM bank. (Can be used as Erase check of each EPROM bank.)
	8	• EPROM is not inserted.

NOTES:

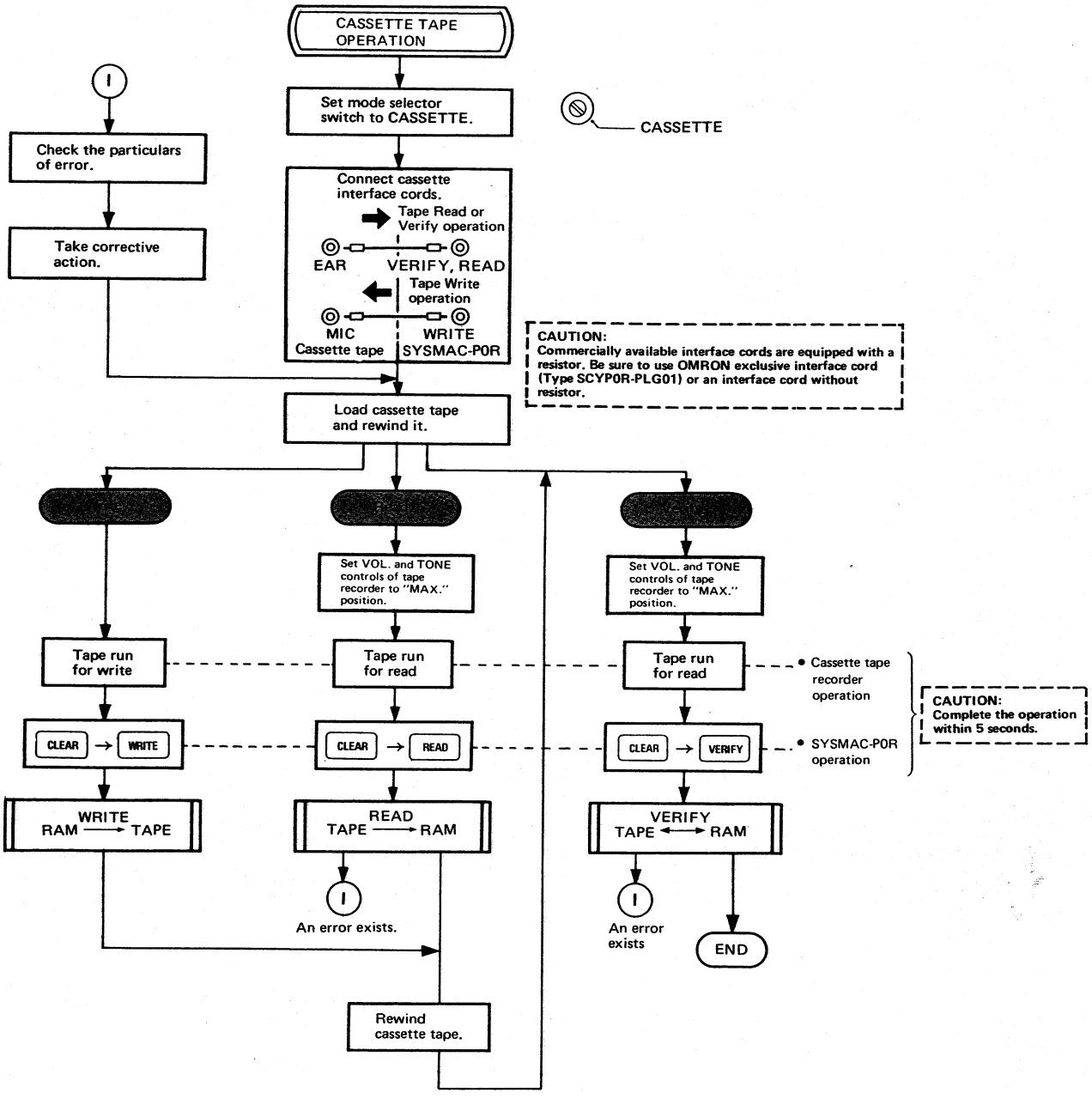
1. Numerics appearing in the ADDRESS display indicates the address where the initial error has occurred.
2. When EPROM Read operation is performed with the EPROM chip inserted upside down, the ERROR indicator does not illuminate, but the data different from the contents of the EPROM will be transferred to the RAM. Therefore, pay attention to the inserted direction of the EPROM chip.
3. To confirm whether or not the specified EPROM bank has been erased, the following key operation is possible.

   CLEAR → Bank designation → VERIFY

   When ERROR indicator illuminates and error message 7 is displayed, it indicates that EPROM has been erased.

6.19 Cassette Tape Handling

As a method of keeping user programs in storage, data may be recorded on a cassette tape by using a commercially available cassette tape recorder.
In the following, a general operational flowchart is shown.



NOTES:
1. Be sure to use a monaural cassette tape recorder.
2. Use a new battery for the cassette tape recorder.
3. Always use a new cassette tape for recording. Note that the presence of scratches or other damage on the tape surface prevents data from being written or read properly.
4. Voltage drop of the battery in the cassette tape recorder results in a decrease in the output level and consequently a failure in signal descrimination.

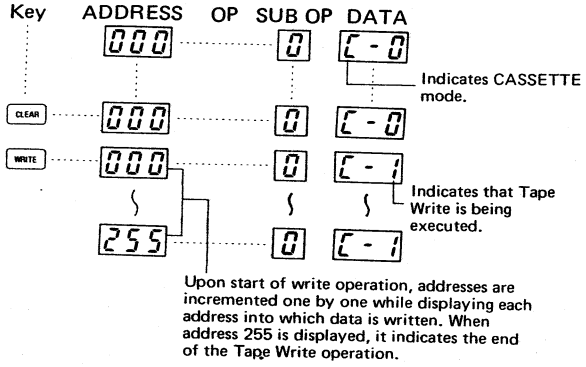
6.20 Tape Write Operation

This operation is to record the contents of the RAM (program memory) on a cassette tape.

- **Operating procedure**

Refer to 6.19 Cassette Handling

- **Display**



NOTES:

1. Upon completion of the Tape Write operation, be sure to perform the Tape Verify operation to confirm that the data have been recorded on the tape properly.
2. Error detection cannot be performed during the Tape Write operation.
   Even if the tape does not run, data will be transferred unilaterally from the RAM. So, be sure to confirm that the tape is running smoothly.
3. If the power is turned off or the cassette is ejected during the Tape Write operation, the tape write will be interrupted. Retry the tape write operation from the beginning.
4. During the Tape Write operation, no PROGRAM key input will be accepted.
5. For the Tape Write operation, use the WRITE → MIC jack to connect one of the cassette tape interface cords. For subsequent verify operation, use VERIFY READ ← EAR jack.

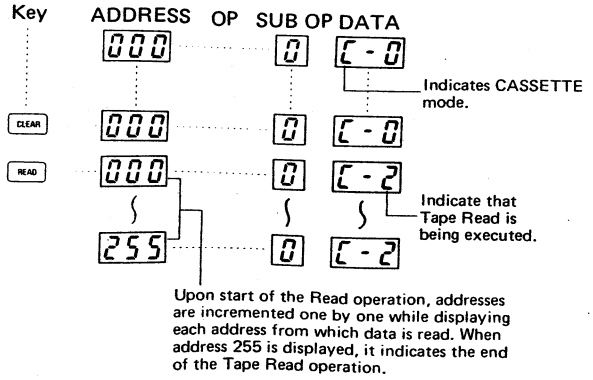
6.21 Tape Read Operation

This operation is to transfer the program data recorded on the cassette tape into the RAM.

- **Operating procedure**

Refer to 6.19, Cassette Tape Handling

- **Display**



NOTES:

1. Upon completion of the Tape Read operation, be sure to perform the Tape Verify operation to confirm that the data have been transferred from the tape to the RAM.
2. If the power is turned off or the cassette is ejected during the Tape Read operation, the tape read will be interrupted. Retry the tape read operation from the beginning.
3. During the Tape Read operation, no PROGRAM key input will be accepted.
4. Be sure to set the volume control and tone control of the cassette tape recorder to maximum.

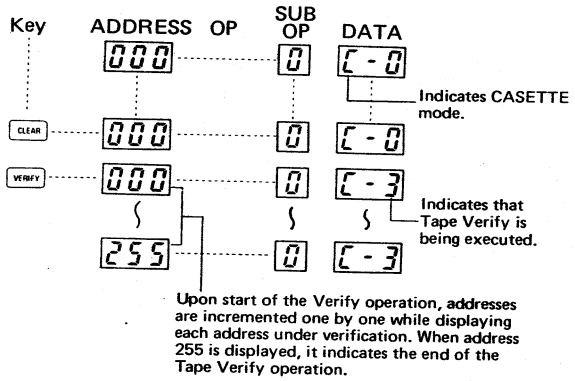
6.22 Tape Verify Operation

This operation is to verify the contents of the RAM against the programmed data recorded on a cassette tape.

- **Operating procedure**

Refer to 6.19 Cassette Handling

- **Display**



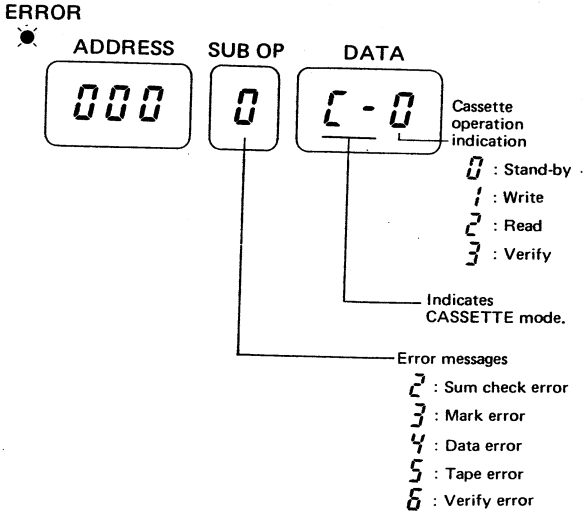
NOTES:

1. If the power is turned off or the cassette tape is ejected during the Tape Verify operation, the tape read will be interrupted. Retry the tape verify operation from the beginning.
2. During the Tape Verify operation, no PROGRAM key input will be accepted.
3. Be sure to set the volume control and tone control of the cassette tape recorder to maximum.

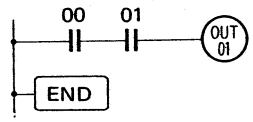
6.23 Errors in Cassette Mode

During a Tape Read, or Verify operation, one of the following error messages appears on the SUB OP display when the ERROR indicator illuminates. The description of each message is shown below.

- **Display**



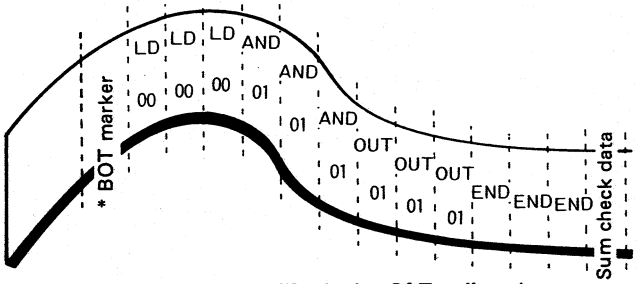
- **Tape data format**



Coding

Address	OP	Sub Operand	Data
000	LD		00
001	AND		01
002	OUT		01
003	END		
⋮			
⋮			

Tape format containing the above circuit data



* BOT marker means the "Beginning Of Tape" marker which identifies the point on a tape at which writing or reading can begin.

- **Errors in tape read operation**

Operation	Error message	Description of message
Tape Read	2	**(SUM CHECK ERROR)** The contents of the cassette tape are read to the end of the program, and the number of logical "1" memory bits composing each instruction is added and checked. If it agrees with the sum check data recorded on the tape during the WRITE operation, the CPU checks whether or not the contents of the tape are correct. If both data do not coincide, the CPU judges that a sum check error exists.
	3	**(MARK ERROR)** On a cassette tape, a BOT (Beginning of tape) marker is recorded at the beginning of the tape in the WRITE operation. If this BOT marker does not appear within a given time after the start of the READ operation, the CPU judges that a mark error exists the tape.
	4	**(DATA ERROR)** When recording data on a cassette tape, the same data (i.e., instruction) is recorded 3 times consecutively. When the three same instructions are read, the CPU checks whether or not all the three data are the same. If two of them do not coincide, the CPU judges that a data error exists.
	5	**(TAPE ERROR)** When recording data on a cassette tape, the same data (i.e., instruction) is recorded 3 times consecutively. When the three same instructions are read, the CPU checks whether or not all the three data are the same. If only one of them does not coincide, the CPU judges that a tape error exists.

- **Errors in tape verify operation**

Operation	Error message	Description of message
Tape Verify	3	**(MARK ERROR)** On a cassette tape, a BOT marker is recorded at the beginning of the tape in the WRITE operation. If this BOT marker does not appear within a given time after the start of the READ operation, the CPU judges that a mark error exists in the tape.
	4	**(DATA ERROR)** When recording data on a cassette tape, the same data (i.e., instruction) is recorded 3 times consecutively. When the three same instructions are read, the CPU checks whether or not all the three data are the same. If two of them do not coincide, the CPU judges that a data error exists.
	5	**(TAPE ERROR)** When recording data on a cassette tape, the same data (i.e., instruction) is recorded 3 times consecutively. When the three same instructions are read, the CPU checks whether or not all the three data are the same. If only one of them does not coincide, the CPU judges that a tape error exists.
	6	**(VERIFY ERROR)** During the Verify operation, if the contents of the cassette tape do not coincide with the contents of the RAM, the CPU judges this condition as a verify error.

6.24 Functions of I/O Checker

The I/O checker is available for user program check and for manual operation of the SYSMAC-P0R.

■ FEATURES

- **Convenient for program debugging**
  Program debugging of the SYSMAC-P0R is possible while it is in the RUN mode by inhibiting external inputs and in turn providing the SYSMAC-P0R with dummy inputs through the switch operation of the I/O checker.
- **Forced output ON/OFF operation is possible.**
  While the SYSMAC-P0R is in the STOP mode, external outputs can be forced to turn on or off with the I/O checker.

■ FUNCTIONS

Connect the I/O checker to the I/O unit connector of the SYSMAC-P0R, and the I/O checker will function as follows.

1. With SYSMAC-P0R in RUN mode

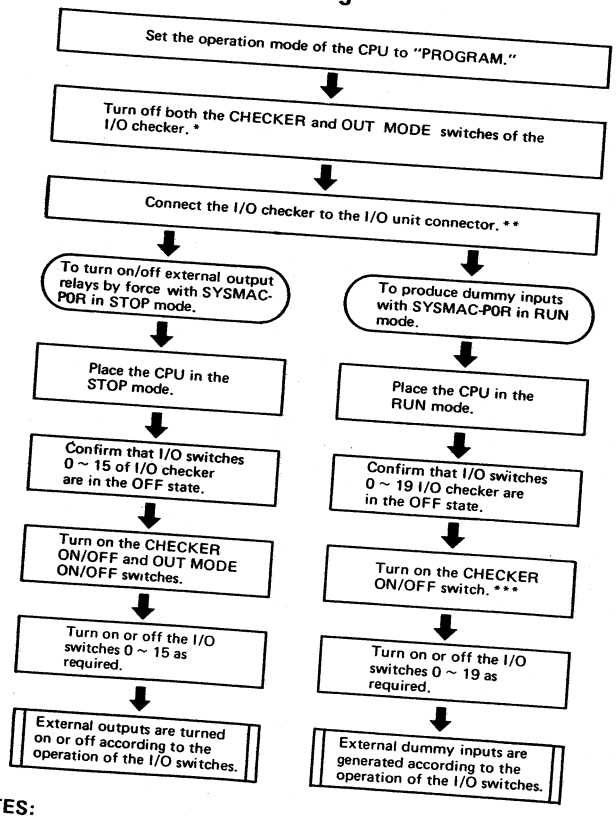
CHECK ER Switch	STOP MODE Switch	Function of SYSMAC-P0R
OFF	ON or OFF	SYSMAC-P0R accepts signals from the external input terminals and ignores input signals from the checker.
ON	ON or OFF	SYSMAC-P0R ignores signals from the external input terminals and accepts the ON/OFF states of the I/O checker switches corresponding to the input terminals of the SYSMAC-P0R as inputs.

2. With SYSMAC-P0R in STOP mode

CHECKER switch	OUT MODE switch	Function
OFF	ON or OFF	SYSMAC-P0R does not operate irrespective of the ON/OFF states of the I/O checker switches.
ON	OFF	Ditto
ON	ON	Output relays can be forced to turn on or off according to the ON/OFF states of the I/O checker switches corresponding to the output relay numbers of the SYSMAC-P0R.

NOTES:
1. The OUT MODE switch is effective only when the SYSMAC-P0R is in the STOP mode. This switch is turned on in the manual operation mode of the SYSMAC-P0R. With this switch turned on, the output relays 00 ~ 15 of the SYSMAC-P0R can be forced to turn on or off.
2. The CHECKER switch supplies power to the I/O checker. However, note that when the cable is connected with this switch on, the I/O checker will not be placed in the ON state if the power is turned off and then on again. In this case, turn off the CHECKER switch once and then turn it on again to place the I/O checker in the ON state.

6.25 I/O Checker Handling



NOTES:
* Even if the I/O checker is connected to the I/O unit connector with the CHECKER and OUT MODE switches turned on, the I/O checker will not operate for protection of external devices. To place the I/O checker in the ON state, the CHECKER switch must be turned OFF once from the ON position and then turned ON again.
** I/O unit connecting connector has an identically designed fitting at each end and can thus be connected from either end.
*** To change the operation mode of the SYSMAC-P0R from "RUN" to "PROGRAM" while it is receiving dummy inputs from the I/O checker, be sure to turn off the CHECKER switch. Outputs can be generated from the I/O checker only when the SYSMAC-P0R is in the STOP mode.

6.26 Cautions in Operating SYSMAC-P0R

When operating the SYSMAC-P0R, pay attention to the following points.

CAUTIONS:
- **Before connecting the CPU with the I/O unit, be sure to turn off the AC power to the SYSMAC-P0R.**
- **Before power application, be sure to set the desired supply voltage using the voltage selector socket with a fuse. (The rated voltage is factory-set to AC 240V prior to shipment.)**
- **The key inserted into the mode selector switch can be removed at either the RUN or STOP position. However, when the key inserted into the mode selector switch is removed at the RUN position, the SYSMAC-P0R is capable of performing such operations as search, monitor, trace, etc.**
- **With the mode selector switch in the STOP position, all the functions of the SYSMAC-P0R are disabled.**

7. Installation and Wiring

The SYSMAC-P0R is a highly reliable programmable controller which is resistant to adverse environmental conditions. However, in order to permit the programmable controller to fully exhibit its functions, as well as to enhance its reliability, care must be exercised on the following points when installing the programmable controller.

7.1 Mounting Locations and Environmental Conditions

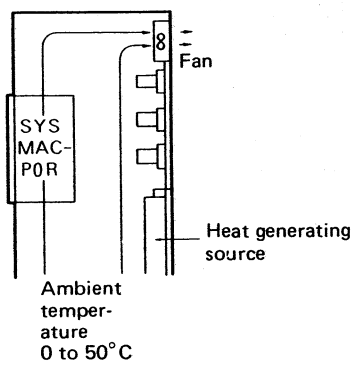
When installing the SYSMAC-P0R programmable controller, avoid the following locations.

- Location where the ambient temperature is beyond the range of 0 to 50°C.
- Location where temperature changes abruptly, thus resulting in condensation.
- Location where relative humidity exceeds the range of 30 to 90%.
- Location subject to corrosive gas or flammable gas.
- Location subject to excessive dust, salt, or iron particles.
- Location subject to vibration and shock.
- Location subject to direct sunlight.

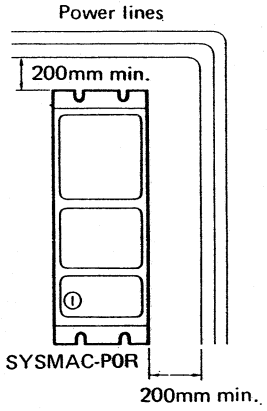
7.2 Mounting Positions within Control Panels

When mounting the SYSMAC-P0R in a control panel, take into consideration the operability, maintenability and environmental resistance of the programmable controller.

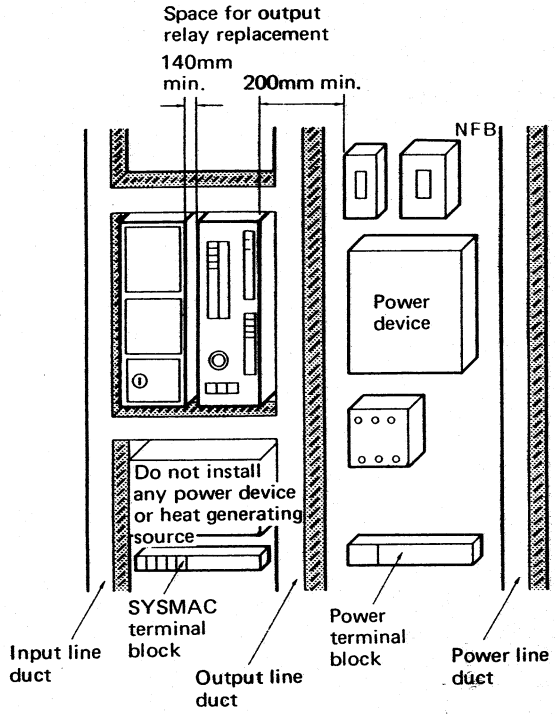
1. To permit the use of the SYSMAC-P0R within the ambient operating temperature range, pay attention to the following points.
   a. Provide the programmable controller with adequate space for ventilation.
   b. Avoid mounting the controller directly above any heat generating sources (heater, transformer, resistor of high capacity).
   c. Install a fan for forced ventilation if the ambient temperature exceeds 50°C.



2. Avoid mounting the SYSMAC-P0R in a panel in which high-tension equipment is installed.
3. Provide a distance of more than 200mm between the high-tension or power lines and the SYSMAC-P0R.



4. Mount the SYSMAC-P0R as far away as possible from high-tension equipment or power devices for the sake of safety in maintenance and operation.



5. Mounting the SYSMAC-P0R at a height 1,000 to 1,600mm above the installed surface of the control panel will facilitate the operation of the programmable controller.

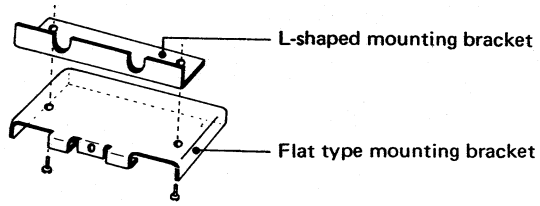
7.3 How to Install within Control Panel

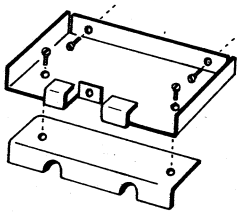
The SYSMAC-P0R can be installed with the I/O unit separated from the CPU, or with both units integrated. The I/O unit and the CPU are connected with a 10-pin flat cable. The flat cable is available in two types; 3m cable (Type SCYP0R-CN300) and 20cm cable (Type SCYP0R-CN020). Be sure to use either of the two OMRON supplied cables.

CAUTION:
Before connecting or disconnecting the flat cable, be sure to turn off the main power source.

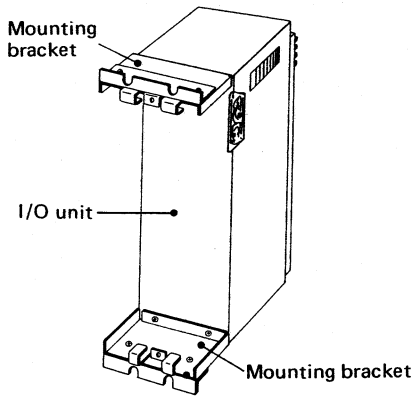
- **Assembly procedure**

1. Assemble a pair of L-shaped mounting brackets with a pair of flat type mounting brackets as shown below.

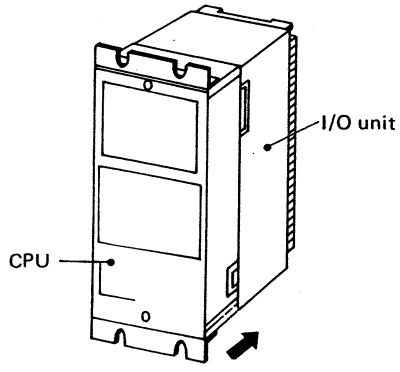




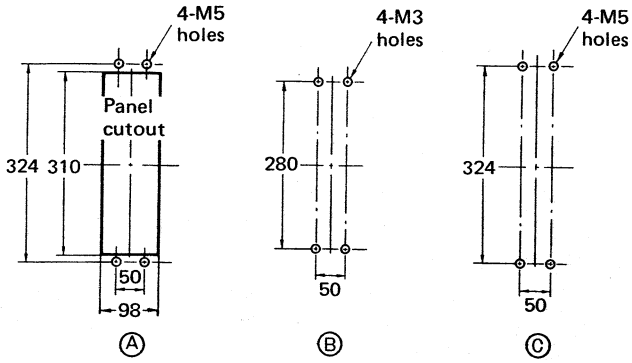
2. Secure the assembled pairs of mounting brackets respectively to the upper and lower parts of the I/O unit.

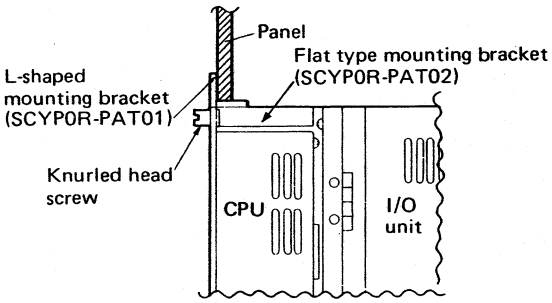


3. Mount the CPU.

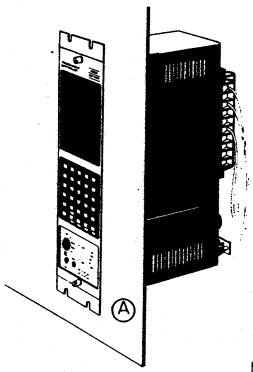


- **Mounting dimensions**

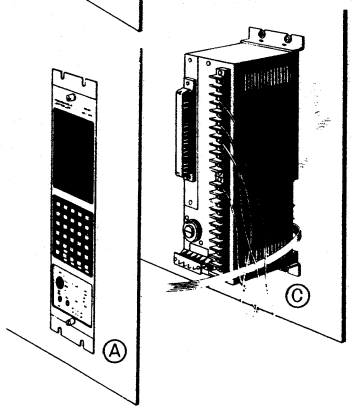




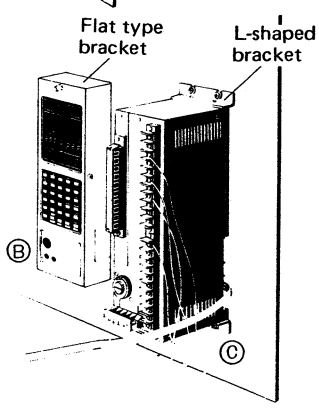
Mounting brackets required for integrated, flush mounting
L-shaped ..... 1 set
Flat type ..... 1 set



Mounting brackets required for separated mounting
L-shaped ..... 2 sets
Flat type ..... 1 set

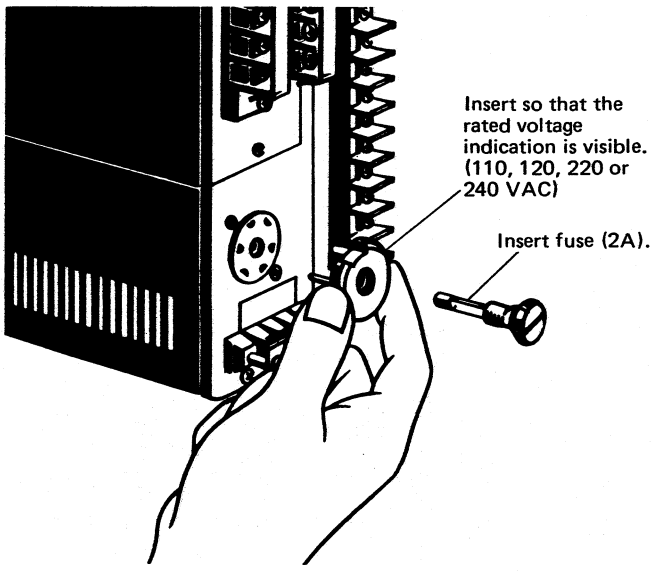


Mounting brackets required for separated mounting
L-shaped ..... 1 set
Flat type ..... 1 set



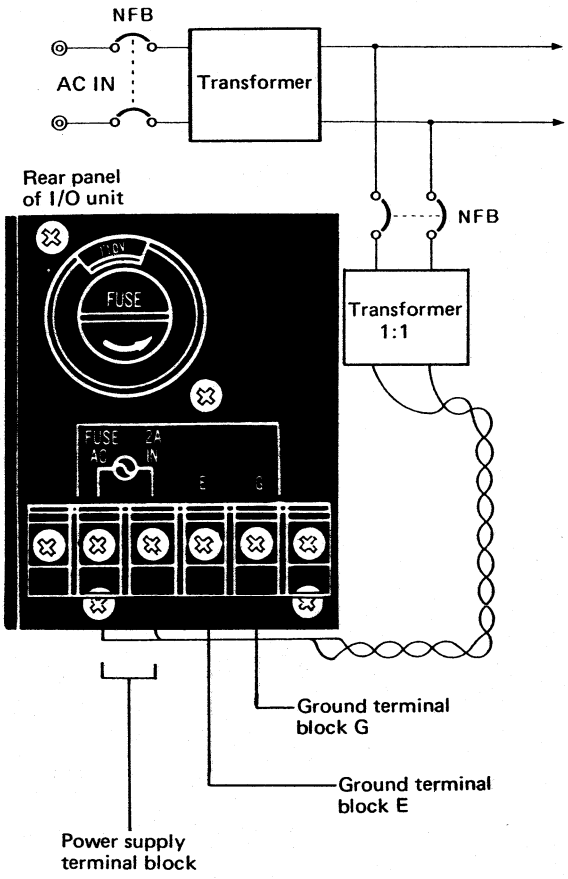
7.4 Processing of Wiring within Control Panel

1. Power supply and wiring
   - Before power application, be sure to set desired supply voltage using the voltage selector socket with a fuse. (The rated voltage is factory-set to AC 240V prior to shipment.)



Voltage Setting Method

- As the power supply line of the SYSMAC-P0R, employ a wire of 2mm^2 min. so as to prevent voltage drop. (Use of twisted pair wires is recommended.)
- For general noise on the power supply line, the noise suppressing circuit in the SYSMAC-P0R is sufficient. However, supplying power through a transformer having a transformer voltage ratio of 1:1 will help reduce equipment-to-ground noise to a great extent and installation of such a transformer is recommended.
  Terminal G of the I/O unit is a ground terminal used for prevention of electric shock. Use an exclusive ground wire (having a conductor cross-sectional area of 2mm^2 min.) for grounding at a grounding resistance of less than 100Ω.
  Terminal E is a noise filter neutral terminal and the grounding is not basically required. In case of a large noise which may cause an erroneous operation, E and G are short-circuited for exclusive grounding (at a grounding resistance of less than 100Ω).



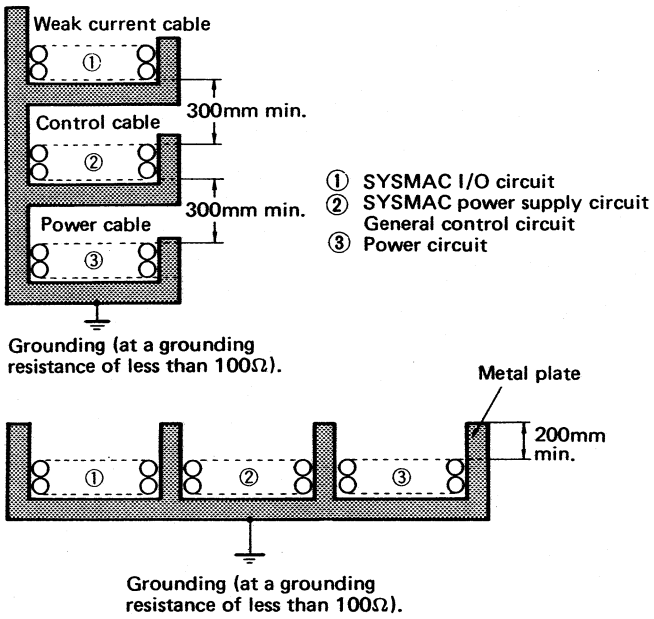
Note that common use of the grounding line with other equipment or connecting to the beam of the building may adversely affect the system.
Keep the length of the ground wire within 20m.
Care must be taken to the grounding resistance as it varies depending on the nature of ground, water content, seasons and the time elapsed after the underground laying of the ground wire.

7.5 Operation at Power Failure

1. As the power supply of the SYSMAC-P0R, supply power within +10%, −15% of the supply voltage.
2. The power sequence circuit is incorporated in the power supply unit of the SYSMAC-P0R to prevent the programmable controller from malfunctioning due to a momentary power failure or a decrease in the supply voltage.
   a. Supply voltage drop
      If the supply voltage drops below its 85%, the alarm buzzer sounds and the operation of the SYSMAC-P0R stops, causing external output relays to turn off.
   b. Momentary power failure
      If a momentary power failure of more than 1 cycle or a voltage drop to less than 85% of the supply voltage occurs, the power failure detecting circuit of the SYSMAC-P0R functions to stop the programmable controller automatically.
   c. Automatic reset
      The SYSMAC-P0R will automatically resume its operation after the supply voltage (more than 85%) is restored.

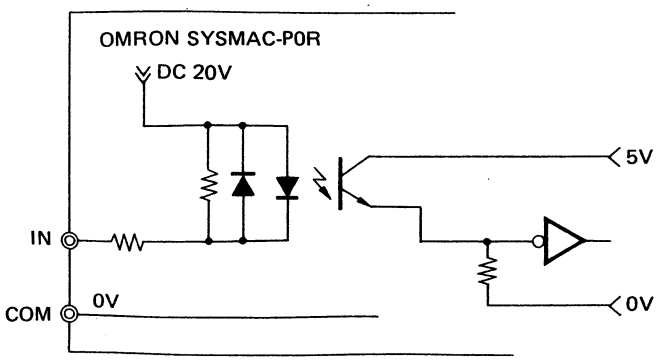
7.6 External Wiring

1. Be sure to process the input/output lines of the SYSMAC-P0R separately from other control lines. (Do not share the conductors of the I/O cable with others.)
2. To process the cables for the SYSMAC-P0R with power cables rated at 400V 10A max. or 220V 20A max.:
   a. Be sure to provide a minimum distance of 300mm between both cables when their racks are paralleled.
   b. Be sure to screen them with a grounded metal plate when both cables are placed in the same duct at the termination process of the cable laying work.

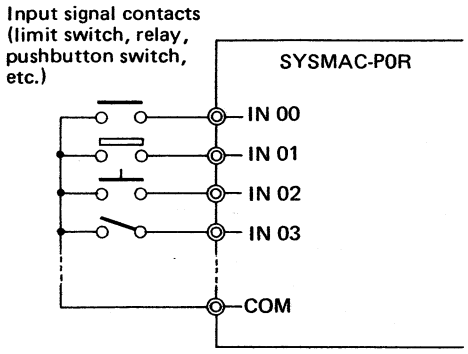


7.7 Output Forms of Input Switches and Methods of Interfacing SYSMAC-P0R

- **Input system: Sink type**
  1. Input characteristics
     Input voltage: DC 20V (unregulated internal power supply)
     Input current: 10mA TYP.
     Input impedance: 1.6kΩ
     Input threshold level: [ON] 5mA min.
     [OFF] 2mA max.
  2. Input circuit diagram

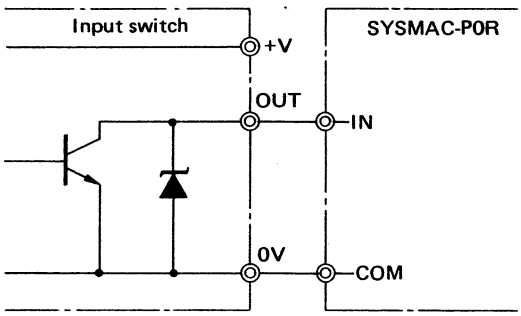


- **In case of contact input:**
  When a contact (no-voltage contact) input is employed, connect one of the input lines to the COM terminal and the others to the IN terminals (00 to 19).

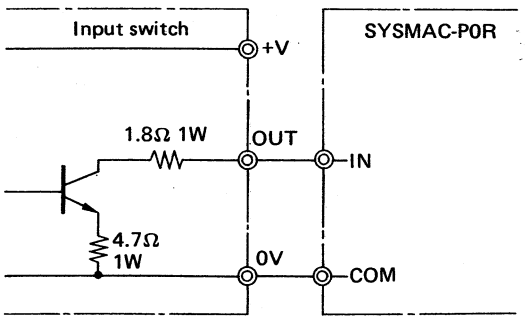


- **In case of solid-state input:**
  When using solid-state input switches, pay attention to the output forms of the respective input switches. The following are examples interfacing with OMRON proximity switches and photoelectric switches.

  1. NPN open collector type: This type can be used.

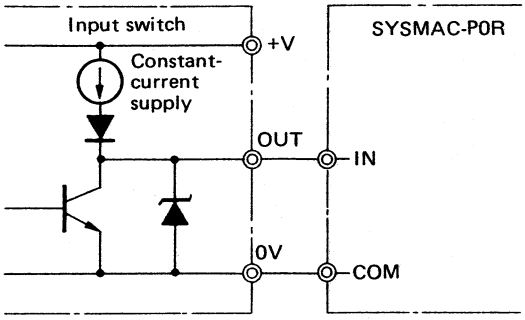


Applicable models
- OMRON proximity switches
  Type TL-XP□(M) series
  (+V: DC 10 to 30V)
  Type E2M-□P□ series
  (+V: DC 24V)



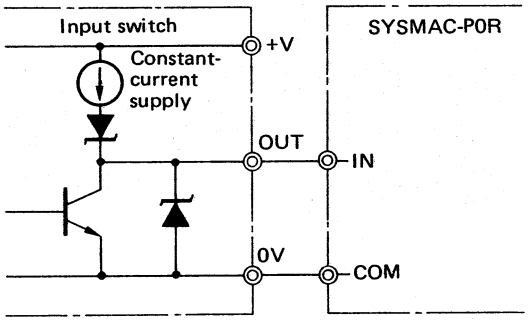
Applicable models
- OMRON proximity switches
  Type TL-LP50
  (+V: DC 10 to 30V)

2. NPN output type: This type can be used.



Applicable models
- OMRON proximity switches
  Type TL-X□E□ series
  (+V: DC 10 to 40V)

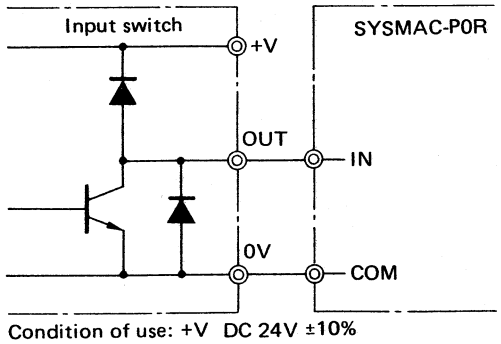
3. NPN output type: This type can be used conditionally.



Condition of use: DC 40V ≧ +V ≧ DC 24V

Applicable models
- OMRON photoelectric switches
  Model E3S series
  Model E3S-L series
  Model E3S-G series
  Model E3S-X series
  Model E3N series
  (+V: DC 12 to 24V)

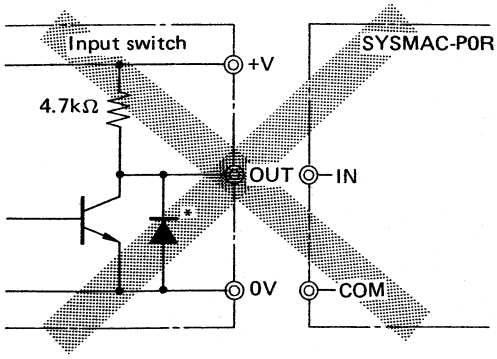
4. NPN output type: This type can be used conditionally.



Condition of use: +V DC 24V ±10%

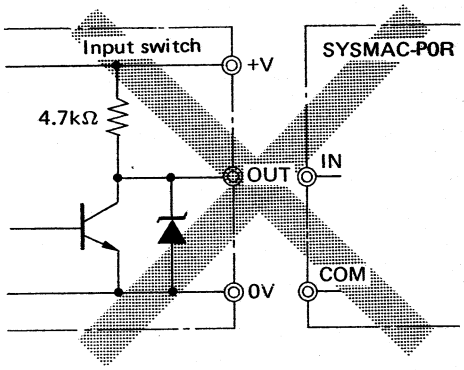
Applicable models
- OMRON proximity switches
  Type TL-P□, TL-PH□ series
  (+V: DC 24V)

5. NPN output type: This type cannot be used.



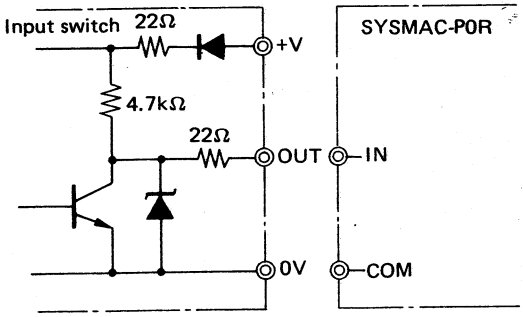
Models not applicable
- OMRON proximity switches
  Type TL-X□ (M) series
  (+V: DC 10 to 14V)
  Type TL-N□/-H□/-F□ series
  (+V: DC 12V)
  Type TL-G□/-Q□ series
  (+V: DC 12V)

NOTE: For Type TL-G□, the diode marked * is not provided, but a capacitor (0.01μF) is incorporated instead.



Models not applicable
- OMRON proximity switches
  Type E2M-□□ series
  (+V: DC 12V)

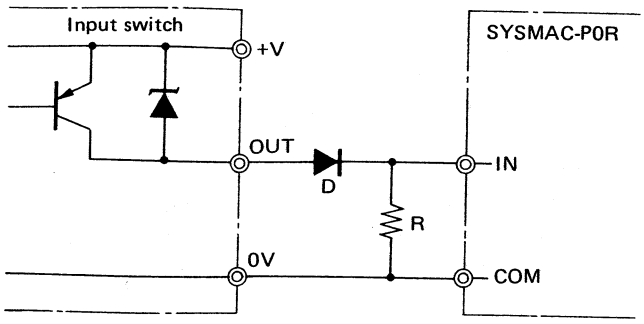
6. NPN output type: This type can be used conditionally.



Condition of use: +V DC 24V ±20%

Applicable models
- OMRON proximity switches
  Type E2K-C25ME□ series
  (+V: DC 10 to 40V)

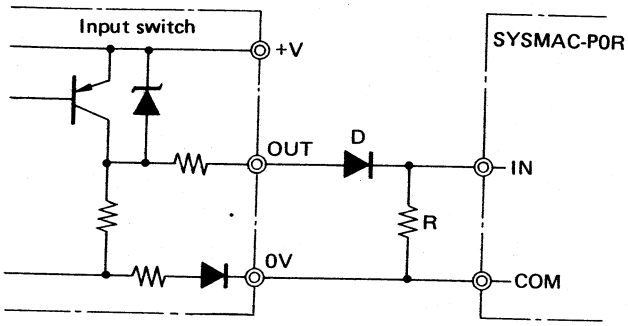
7. PNP open collector type: This type can be used conditionally.



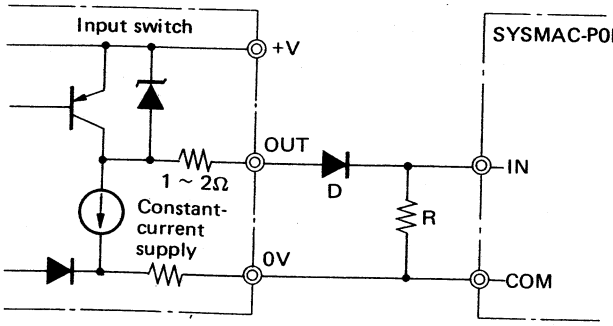
Condition of use: D: Capacity must be 30mA min.
R: 1kΩ, 2W
DC 40V ≧ +V ≧ DC 24V

Applicable models
- OMRON proximity switches
  Type TL-XP□P(M) series
  (+V: DC 10 to 30V)

8. PNP output type: This type can be used conditionally.



Applicable models
- OMRON proximity switches
  Type E2K-C25MF□ series
  (+V: DC 10 to 40V)



Condition of use: D: Capacity must be 30mA min.
R: 1kΩ, 2W
DC 40V ≧ +V ≧ DC 24V

Applicable models
- OMRON proximity switches
  Type TL-X□F□ series
  (+V: DC 10 to 40V)

For the methods of interfacing described in 3, 4, 7 and 8 as the types that can be used conditionally, if difficult to use, and in 5 and 6 as the types that cannot be used, interface the SYSMAC-P0R with the solid-state input switches through contact input as follows.

One way is to use the contact output of the OMRON Model S3S controller unit for OMRON proximity and photoelectric switches and the other to use an electromagnetic relay.

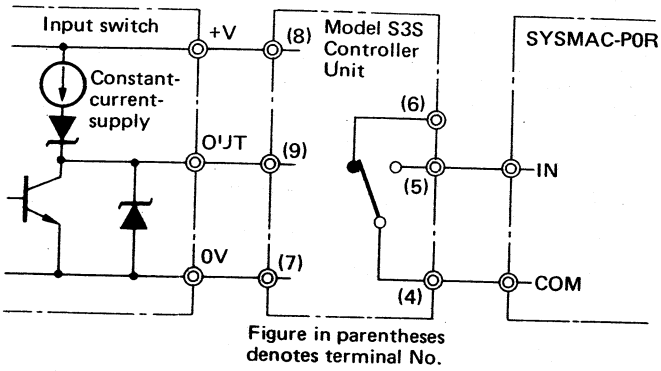
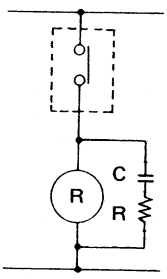


Figure in parentheses denotes terminal No.

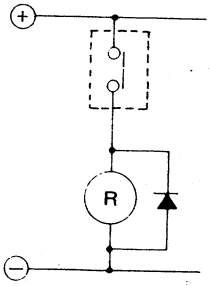
7.8 Hints on Use of Output Contacts

- If any electrical devices, which are likely to generate electric noise, are to be employed as the output loads of the SYSMAC-P0R, be sure to take measures to absorb such noise. For example, electromagnetic relays, valves, etc. generating a noise of 1,200 to 1,300V minimum are subject to noise suppression. For AC operated noise sources, connect a surge suppressor in parallel with the coil of each device. For DC operated noise sources, connect a diode in parallel with the coil of each device.



AC power source

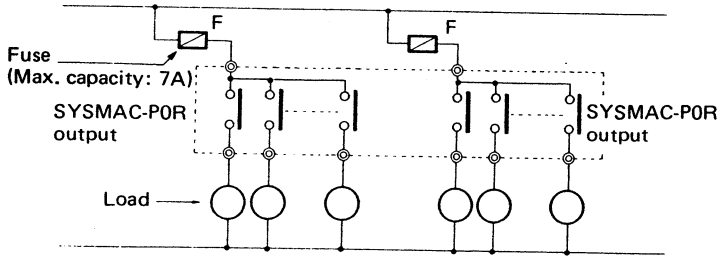
C: 0.5μF ±20% min.
Nonpolarity
Withstand voltage: 1,500V min.
R: 50Ω ±30%, 0.5W



DC power source

Select a diode with the breakdown voltage and current ratings according to the load.

- Since the output contacts (SPST-NO) of the SYSMAC-P0R consist of relay contacts which are packaged on a printed circuit board and connected to the terminal board, short-circuiting any of loads connected to the output contacts may result in the burning of, and consequent damage to, the P.C. board. Therefore, use of fuses is recommended for protection of the output contacts.



8. Maintenance and Inspection

To sustain the proper system operation at all times, it is necessary to inspect the SYSMAC-P0R daily. If any trouble occurs in the SYSMAC-P0R, how the system should be protected and how soon it can be recovered from the failure become important. In this chapter, the items to be inspected on the SYSMAC-P0R and the actions to be taken if the SYSMAC-P0R fails are described.

8.1 Inspection

To make the most of the functions of the SYSMAC-P0R under the best condition, it is necessary to inspect the SYSMAC-P0R daily or periodically.

■ INSPECTION ITEMS

The SYSMAC-P0R employs semi-conductors as its main component elements and has little or no supplies with a limited service life. However, the semi-conductors may deteriorate depending on the environmental conditions and must therefore be inspected periodically. The standard inspection cycle is 6 months to 1 year. According to the environmental conditions, it is recommended to advance the date of inspection. As a result of the daily or periodical inspection, if the SYSMAC-P0R is found to be outside the criteria in the following table, be sure to correct the SYSMAC-P0R so that it falls within the prescribed criteria.

1	AC power supply (a) Voltage (b) Fluctuation	(1) Is the rated voltage available when measured within the CPU rack and at the AC input terminal block?	AC 110, 120, 220, or 240V +10%, −15%
		(2) Does a momentary power failure occur frequently or is there any sharp rise or drop in the supply voltage?	The supply voltage must be within the permissible fluctuation range described above.
2	Environmental conditions (a) Ambient temperature (b) Humidity (c) Vibration (d) Dust, etc.	Are the temperature and humidity within the ranges respectively? (When the SYSMAC-P0R is installed in a control panel, the temperature within the panel may be regarded as the ambient temperature of the programmable controller.	(a) 0 to +50°C (b) 30 to 90% RH (c) Must be free from vibration (d) Must be free from dust
3	Mounting conditions	(1) Are the I/O unit and CPU secured firmly?	The mounting screws must not be loose.
		(2) Are the flat cables for connection of the I/O unit and CPU inserted completely?	The flat cables must not be loose.
		(3) Is there any loose screw in the external wiring?	The screw terminals must not be loose.
		(4) Is there any broken cable in the external wiring?	Ther external wiring must be free from any abnormalities in the appearance.
		(5) Is there any broken conductor in the flat cable?	The flat cable must be free from any abnormalities in the appearance.
4	Service life	(1) Output relays in the I/O unit	Replace with new ones if defective.
		(2) Battery	2 years

CAUTION:
Be sure to turn off the power before replacing any unit (CPU orI/O unit) of the SYSMAC-P0R.

■ NOTES ON INSPECTION

1. If a defective unit is discovered and replaced, confirm whenever or not the replaced unit is abnormal.
2. In the event of a faulty contact of the flat cable, wipe the connector pins with a clean all-cotton cloth moistened with industrial alcohol. Be sure to plug in the flat cable after removing the cloth waste.

■ TOOLS AND TESTING EQUIPMENT REQUIRED FOR MAINTENANCE

In the maintenance of the SYSMAC-P0R, the following tools and testing equipment will facilitate the daily or periodic inspection of the programmable controller.

1. Tools and testing equipment recommended as mandatory equipments
   - Screwdrivers (Phillips and round blade)
   - Tester or digital voltmeter
   - Industrial alcohol and all-cotton cloth
2. Measuring instruments recommended only if required.
   - Synchroscope
   - Pen-recording oscilloscope

■ MAINTENANCE PARTS

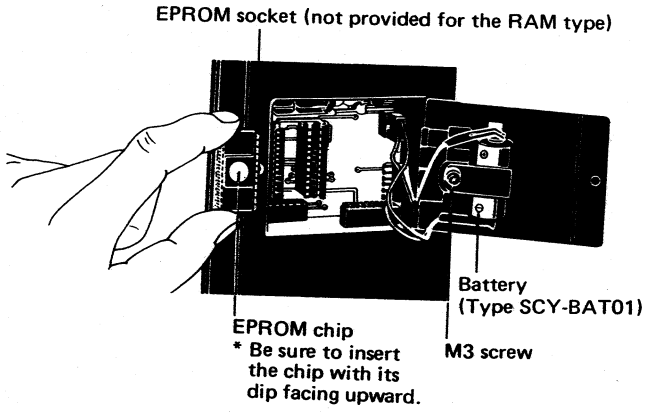
1. I/O unit (Type SCYP0R-I/O01)
   If the SYSMAC-P0R fails, its repair is impossible without any spare parts no matter how early the trouble is discovered. So, it is recommended to have at least one I/O unit as the spare part.
2. Battery (Type SCY-BAT01)
   In general, the service life of a battery is regarded as the time when the capacity of the battery is reduced to 50% of its nominal capacity. The service life of a battery varies greatly depending on the ambient temperature of the battery, depth of discharging, discharge current, etc. With the SYSMAC-P0R, the life of the built-in battery is considered to be 2 years. Therefore, replace the battery with a new one every 2 years.
3. AC power fuse: Rated at 2A

8.2 Replacement of Battery

Be sure to replace the battery within 5 minutes.

- **Procedure:**

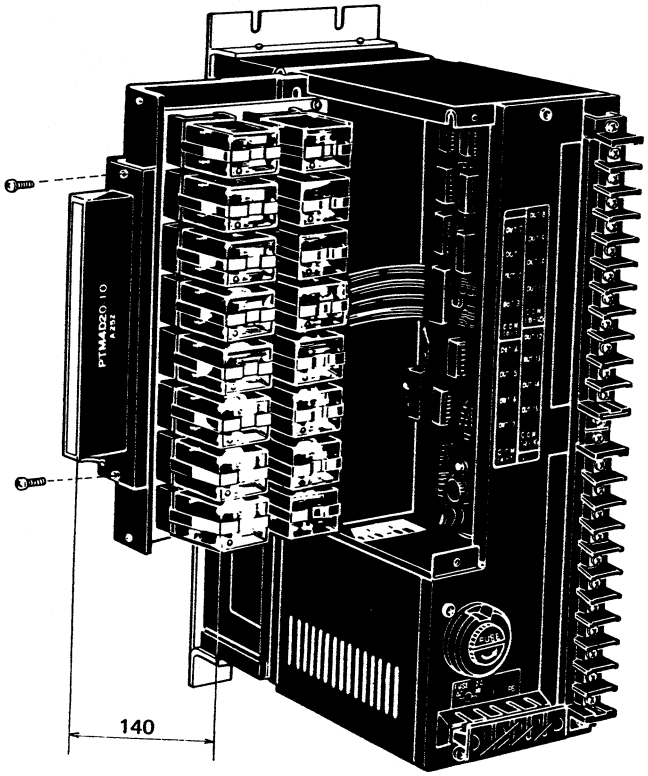
1. Prepare the replacement battery.
2. Turn off the AC power.
3. Remove the screw on the rear panel of the CPU and open the door as shown below.
4. Remove the M3 screw securing the battery and unplug the battery connector.
5. Plug in the connector of the new battery and then replace the battery.
6. Close the door, and secure it with the screw.
7. When the AC power is applied, the battery starts operating.



NOTE: When the AC power is not ON at the time of battery replacement, first apply the AC power for more than 10sec and then turn it off.

8.3 Replacement of Relays

- **I/O unit**

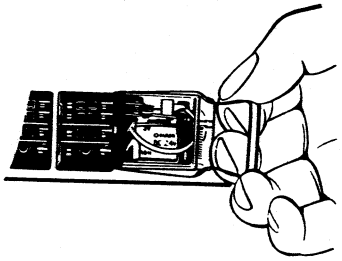


NOTES:

1. Output relays can be replaced easily by removing the two screws as shown above.
2. A space of approx. 140mm is required on the left side of the I/O unit, for relay replacement.
3. Use OMRON Type MY2 (-US) rated at DC 24V as replacement relays. Turn off the power supply when replacing output relays.
4. The OMRON Type MY2 relay is interchangeable with the OMRON Type G3F-203S solid-state relay. When the solid-state relays are desired as output relays due to the requirement to switch loads at high frequency, use the Type G3F-203S relays in place of the Type MY2 relays. In this case, however, only the output terminal numbers 53, 54, 55, 59, 60, 61, 65, 66, 67, 70, 71, 72, 73, 77, 78, 79, 83, 84, 85, 89, 90, 91, 95, 96 and 97 are applicable. The output specifications of the Type G3F-203 relays are as follows:

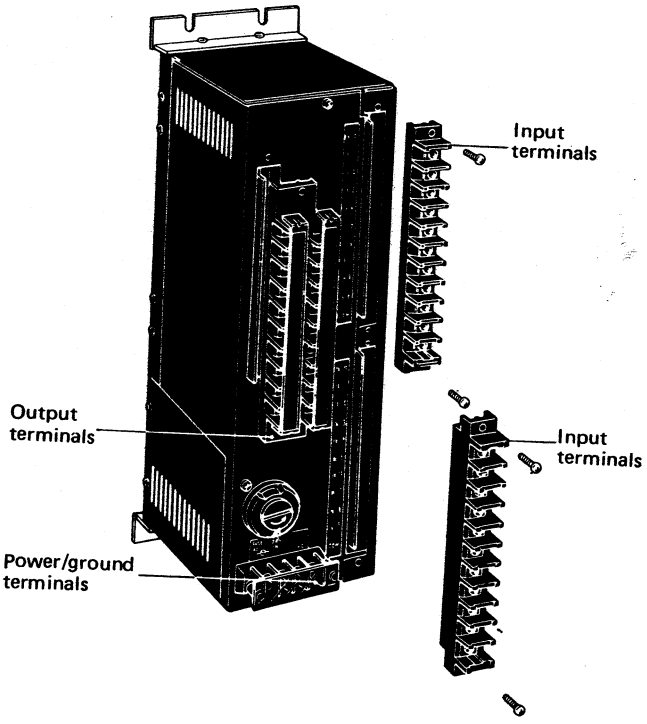
Max. permissible load	75 to 250 VAC, 2A
Operate and release times	Zero cross applied
Leakage current	5mA max. (at 100 VAC) 10mA max. (at 200 VAC)

NOTE: Since one common terminal permits connection of 3 output points, be sure to limit the current flowing through the common terminal to less than 4A.



8.4 How to Remove Terminal Block Connectors

- **I/O unit**



NOTE: Two input terminal blocks and one output terminal block are respectively secured to the I/O unit with two screws and are removable from the I/O unit. Therefore, it is unnecessary to disconnect the I/O wiring when replacing output relays, or reinstalling the I/O unit.

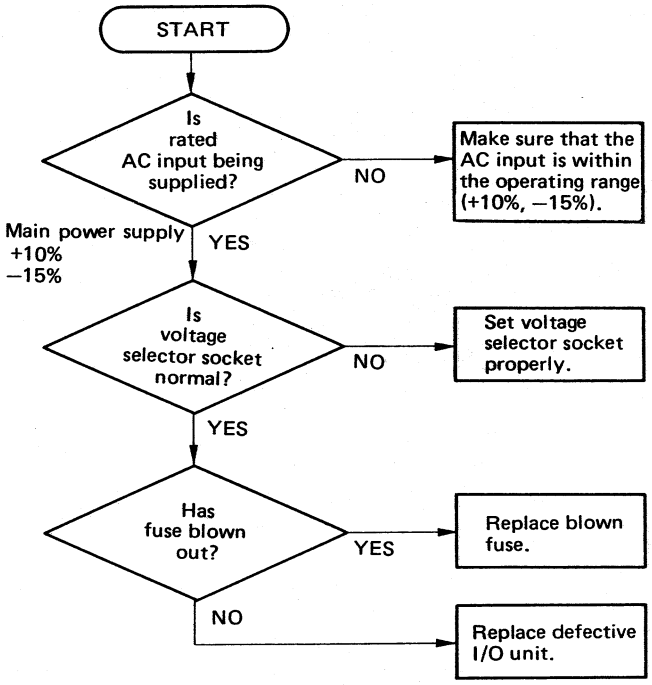
8.5 Troubleshooting

If any abnormality occurs in the SYSMAC-P0R, thoroughly grasp the condition of trouble, check whether the symptom is reproducible or is caused through relationship with other equipment, and then follow the troubleshooting flowcharts shown below.

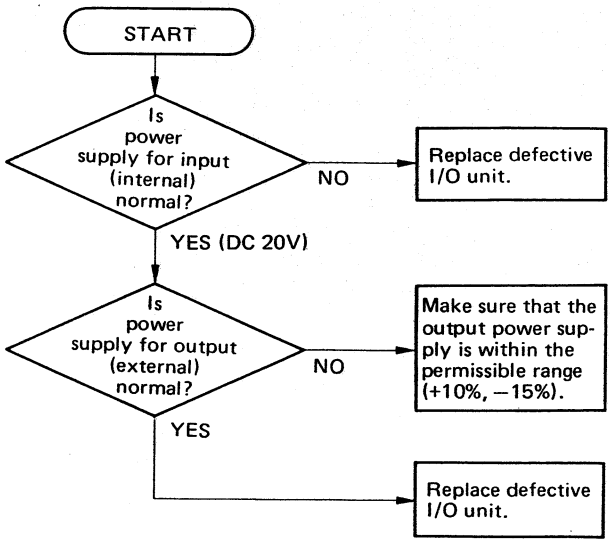
■ I/O UNIT

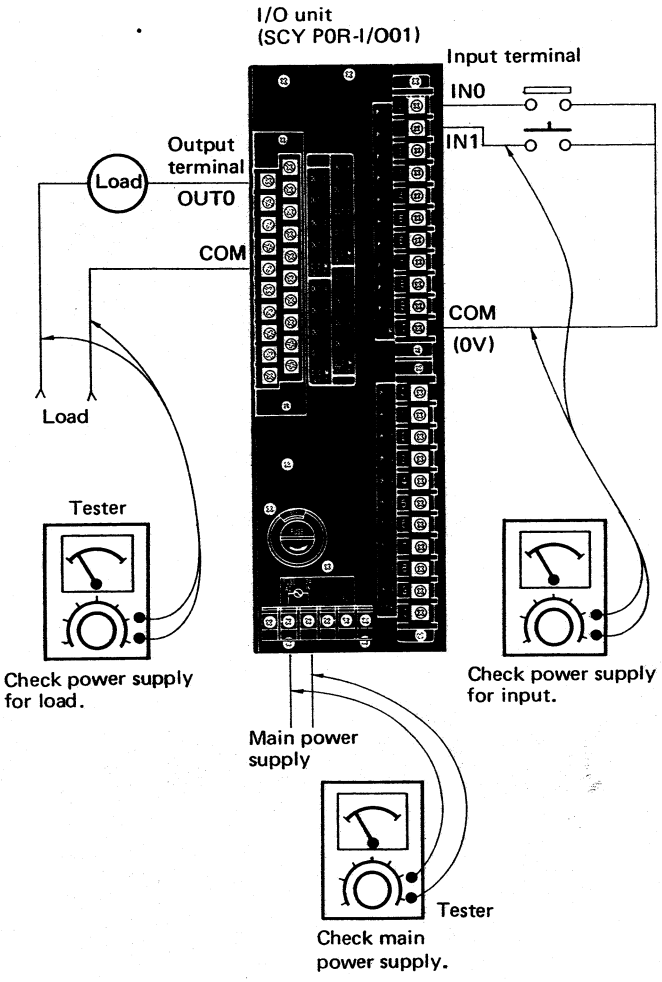
- **Main power supply check**

In this check, the AC power being supplied to the SYSMAC-P0R is confirmed if it is within the specified operating range.

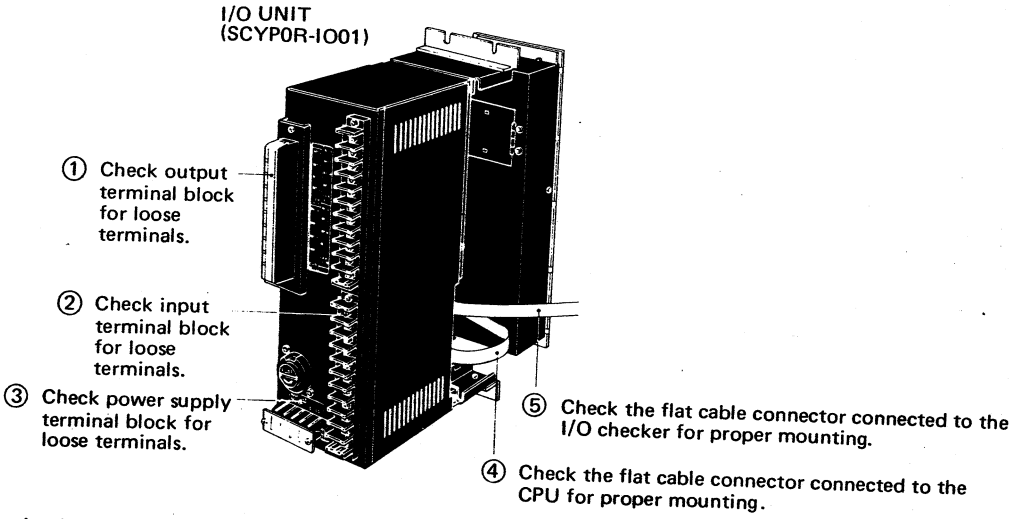


- **I/O device related power supply check**





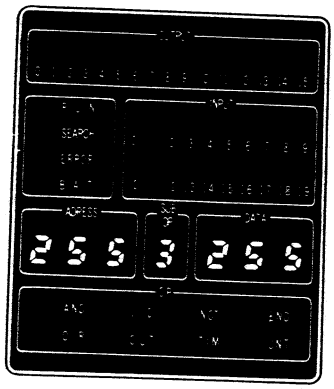
- **Loose terminal check**

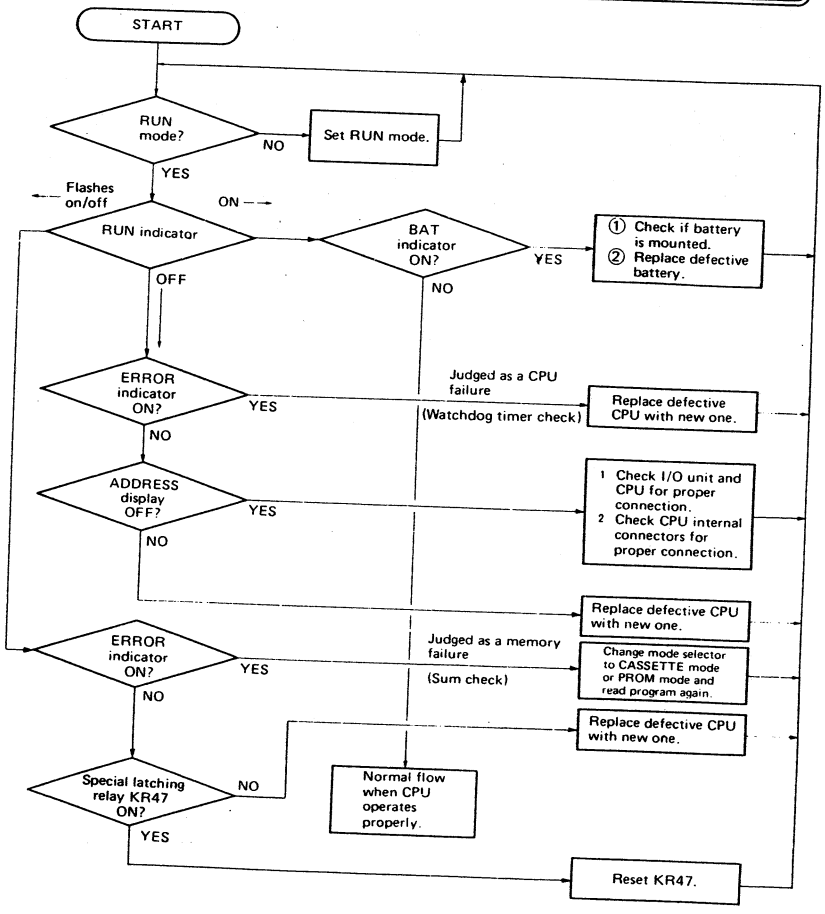


NOTE: The CPU connecting flat cable and I/O checker connecting cable may be connected to either the top or bottom side of the I/O unit connector.

■ CPU

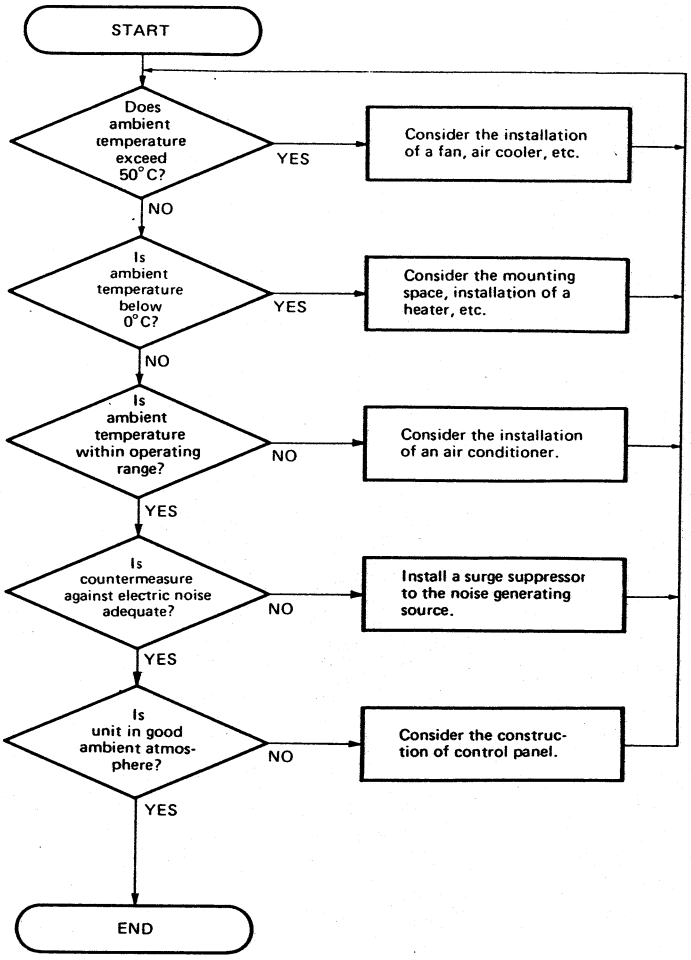
When the CPU is normally operating, the RUN indicator lights, INPUT/OUTPUT indicators are ON or OFF according to the operation of each input/output, and the ADDRESS display indicates "000."
The following flowchart applies to the CPU if abnormality occurs in the unit while it is in the RUN mode.





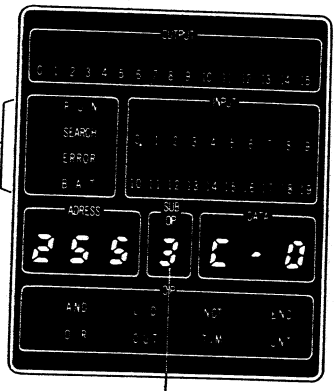
■ EXTERNAL ENVIRONMENTS

Confirm that the SYSMAC-P0R satisfies the environmental requirements described in Section 2.3, Specifications.



■ LIST OF ERROR MESSAGES

An error message appears in the sub OP code display as shown on the right.



Item / Mode	Symptom	Description of check/ Condition of trouble	RUN indicator	ERROR indicator	BATTERY FAULT indicator	State of ALARM relay	SUB OP code
RUN mode	No END instruction	Check the presence of END instruction at the end of a program.	●	●			9
	Memory failure	Sum check	◐	●		MR63 ON	
	Battery failure	Rated battery voltage and battery mounting check	●		●	MR62 ON	
	CPU failure	Watchdog timer check		●			
Program mode	No END instruction	Check the presence of END instruction at the end of a program.		●			9
	Duplicate coil number	Check coil numbers for duplication.		●			C
	Circuit error	Check the ladder diagram for proper circuit configuration or syntax.		●			U
Cassette mode	Memory error	Sum check		●			2
	Mark error	Faulty cassette tape recorder or incomplete tape rewind.		●			3
	Data error	An abnormality occurs during program write into the tape, or the tape is defective due to deterioration.		●			4
	Tape error	Ambiguous data exist in the tape. Rewrite programs into the tape.		●			5
	Verify error	The contents of the tape do not coincide with those of the RAM.		●			6
EPROM mode	Verify error	The contents of the RAM do not coincide with those of the EPROM.		●			6
	Erase error	EPROM contains no data. (Erase check)		●			7
	Read error	EPROM chip not inserted.		●			8

● denotes that the indicator illuminates.
◐ denotes that the indicator flashes.

I/O TERMINAL ASSIGNMENT TABLE FOR OMRON SYSMAC-P0R

Name		Model	Prepared by:	Inspected by:	Approved by:
Customer	Installation location	Drawing No. (Chip No.)			

Input			Output		
Terminal No.	Relay No.	Description of signal	Terminal No.	Relay No.	Description of signal
IN0	00		OUT0	OUT00	
IN1	01		OUT1	OUT01	
IN2	02		OUT2	OUT02	
IN3	03		OUT3	OUT03	
IN4	04		COM		
IN5	05		OUT4	OUT04	
IN6	06		OUT5	OUT05	
IN7	07		OUT6	OUT06	
IN8	08		OUT7	OUT07	
IN9	09		COM		
COM			OUT8	OUT08	
IN10	10		OUT9	OUT09	
IN11	11		OUT10	OUT10	
IN12	12		OUT11	OUT11	
IN13	13		COM		
IN14	14		OUT12	OUT12	
IN15	15		OUT13	OUT13	
IN16	16		OUT14	OUT14	
IN17	17		OUT15	OUT15	
IN18	18		COM		
IN19	19				
COM					

OMRON SYSMAC-P0R CODING SHEET

Name		Model	Prepared by:	Inspected by:	Approved by:
Customer	Installation location	Drawing No. (Chip No.)			

Address	OP	Sub OP	Data	Address	OP	Sub OP	Data	Address	OP	Sub OP	Data	Address	OP	Sub OP	Data
000				064				128				192			
001				065				129				193			
002				066				130				194			
003				067				131				195			
004				068				132				196			
005				069				133				197			
006				070				134				198			
007				071				135				199			
008				072				136				200			
009				073				137				201			
010				074				138				202			
011				075				139				203			
012				076				140				204			
013				077				141				205			
014				078				142				206			
015				079				143				207			
016				080				144				208			
017				081				145				209			
018				082				146				210			
019				083				147				211			
020				084				148				212			
021				085				149				213			
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058				122				186				250			
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061				125				189				253			
062				126				190				254			
063				127				191				255			